

PROTECTION PRODUCTS
10/100 Ethernet Protection

10/100 Ethernet ICs are vulnerable to damage from electrostatic discharge (ESD). The fatal discharge may originate from a charged cable or a "human body". Furthermore, devices used in telecommunications equipment may be exposed to lightning induced transients. This application note illustrates a protection circuit suitable for use in 10/100 Ethernet applications.

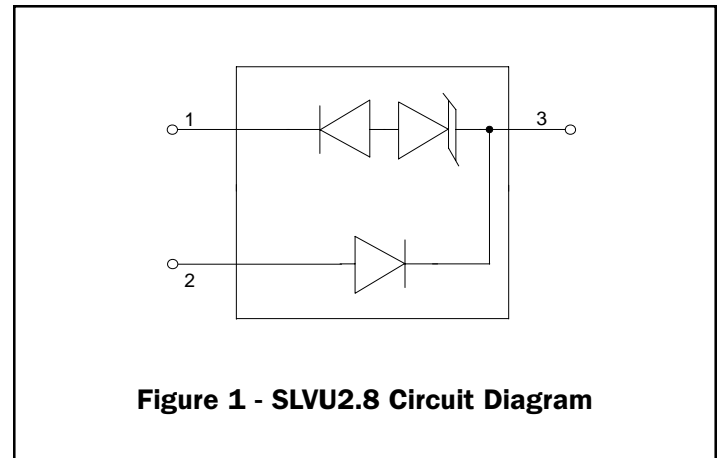
10/100 Ethernet Protection Topology

The Ethernet market is moving from 10 Base-T operating at 10MHz to 100Mbps fast Ethernet. The original 10Base-T Ethernet chips were fairly large geometry CMOS products and they were not very sensitive to static over-voltage. Newer 10/100 Ethernet devices however have become extremely sensitive to latch-up or damage as IC manufacturers have moved to 0.35-micron and smaller line widths. Devices used in Ethernet switches and routers are also exposed to high-energy lightning induced transients.

In a typical system, the twisted-pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver. The transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmit or receive line pair and is capacitively coupled through the transformer to the Ethernet chip. The challenge is to find a TVS (transient voltage suppressor) that will clamp low enough as to prevent latch-up or damage to the Ethernet IC. Also, the protection device must add minimal loading capacitance as high parasitic capacitance can cause significant degradation to the 100Mbps signal.

The Semtech SLVU2.8 is designed to meet the above criteria. The SLVU2.8 circuit diagram is shown in Figure 1. The device features a low voltage TVS diode and a low capacitance compensation diode in the same (SOT-23) package. The TVS diode is constructed using a proprietary EPD process technology yielding a device with superior electrical characteristics at an operating voltage of 2.8V. The series compensation diode acts to reduce the loading capacitance to typically <5pF (pin 1 to 2).

Protection is achieved by connecting two SLVU2.8's in anti-parallel across each line pair. In portable systems, it may be sufficient to provide ESD protection on the sensitive transmit lines (Figure 2). In telecommunica-

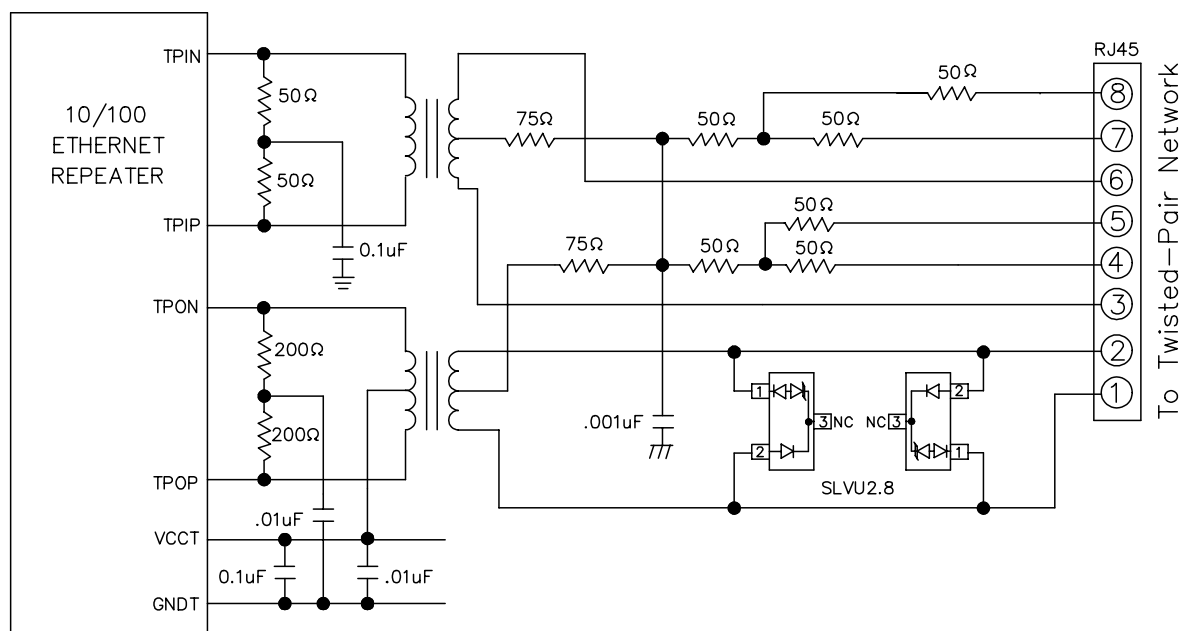
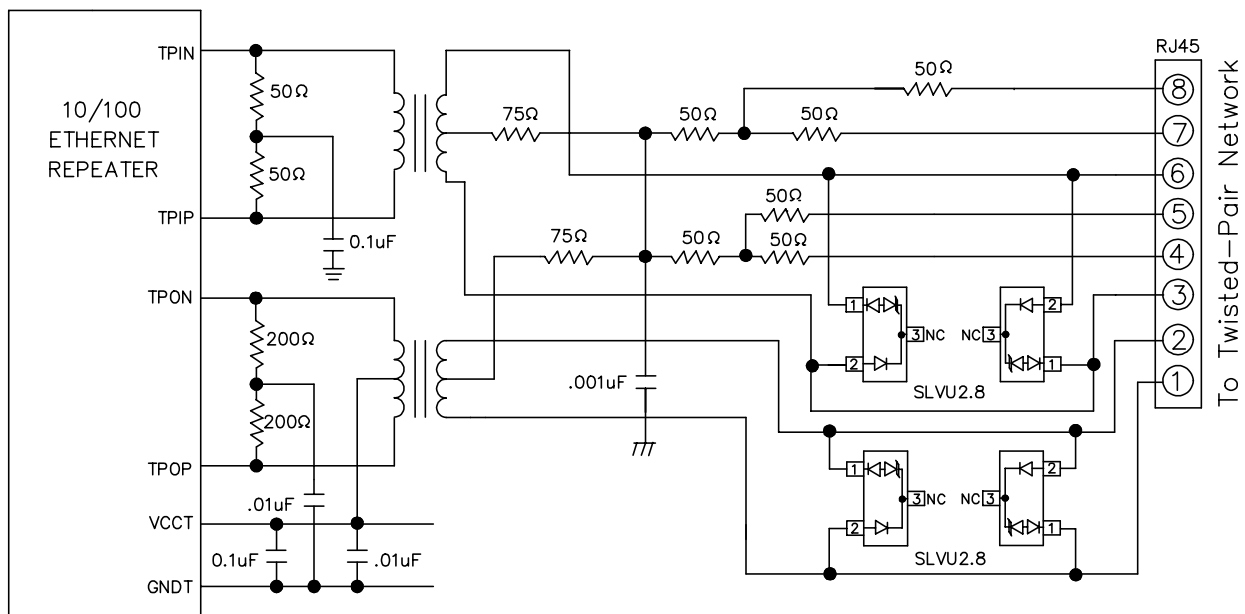

Figure 1 - SLVU2.8 Circuit Diagram

tions applications, the threat of lightning & static discharge requires both transmit & receive line pairs to be protected (Figure 3). The devices are connected in a low capacitance configuration. Two devices are required to provide bidirectional protection. Pin 1 of the first device is connected to line 1 and pin 2 is connected to line 2. Pin 2 of the second device is connected to line 1 and pin 1 is connected to line 2 as shown. Pin 3 **must** be left open on both devices. During negative duration transients, the first device will conduct from pin 2 to 1. The steering diode conducts in the forward direction while the TVS will conduct in the reverse direction. During positive transients, the second device will conduct in the same manner. In this configuration, the total loading capacitance is the sum of the capacitance (between pins 1 and 2) of each device (typically <10pF).

(Update: The SLVU2.8-4 and SR2.8 are also available for 10/100 Ethernet protection. Consult specific data sheets for details.)

Board Layout Considerations For ESD Protection

Board layout plays an important role in the suppression of extremely fast rise-time ESD transients. Recall that the voltage developed across an inductive load is proportional to the time rate of change of current through the load ($V = L di/dt$). The total clamping voltage seen by the protected load will be the sum of the TVS clamping voltage and the voltage due to the parasitic inductance ($V_{C(TOT)} = V_C + L di/dt$). *Parasitic inductance in the protection path can result in significant voltage overshoot, reducing the effectiveness of the suppression circuit.* An ESD induced transient for

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Figure 2 - 10/100 Ethernet Protection Circuit (Transmit Line Pairs Only)

Figure 3 - 10/100 Ethernet Protection Circuit (Transmit & Receive Line Pairs)

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example reaches a peak in approximately 1ns. For a 30A pulse (per IEC 1000-4-2 Level 4), 1nH of series inductance will increase the effective clamping voltage by 30V ($V = 1 \times 10^{-9} (30/1 \times 10^{-9})$). For maximum effectiveness, the following board layout guidelines are recommended:

- Minimize the path length between the SLVU2.8 and the protected line.
- Place the SLVU2.8 near the RJ45 connector to restrict transient coupling in nearby traces.
- Minimize the path length (inductance) between the RJ45 connector and the SLVU2.8.

Meeting Bellcore GR-1089 Intra-Building Requirements

A different design approach is utilized for systems that must meet the intra-building lightning immunity requirements of Bellcore 1089 (Table 1). The SLVU2.8 is not designed to dissipate the required surge. For this application, the LC03-6 is used absorb the metallic

mode surges. Transformers with a minimum isolation voltage of 1500V will provide sufficient protection for the common mode surges.

Surge	Min. Voltage [Vpk]	Rise/Decay Time μ s	Min. Current [A]	Repetitions Each Polarity
1. M	800	2/10	100	1
2. L	1500	2/10	100	1

Notes:

L = Longitudinal Mode, M - Metallic Mode

1 Pulse is a double exponential waveform

2 8/20 μ s s.c. current waveform may be substituted with the inclusion of appropriate series resistance per Bellcore 1089.

Table 1 - GR-1089 Intra-building Lightning Surges

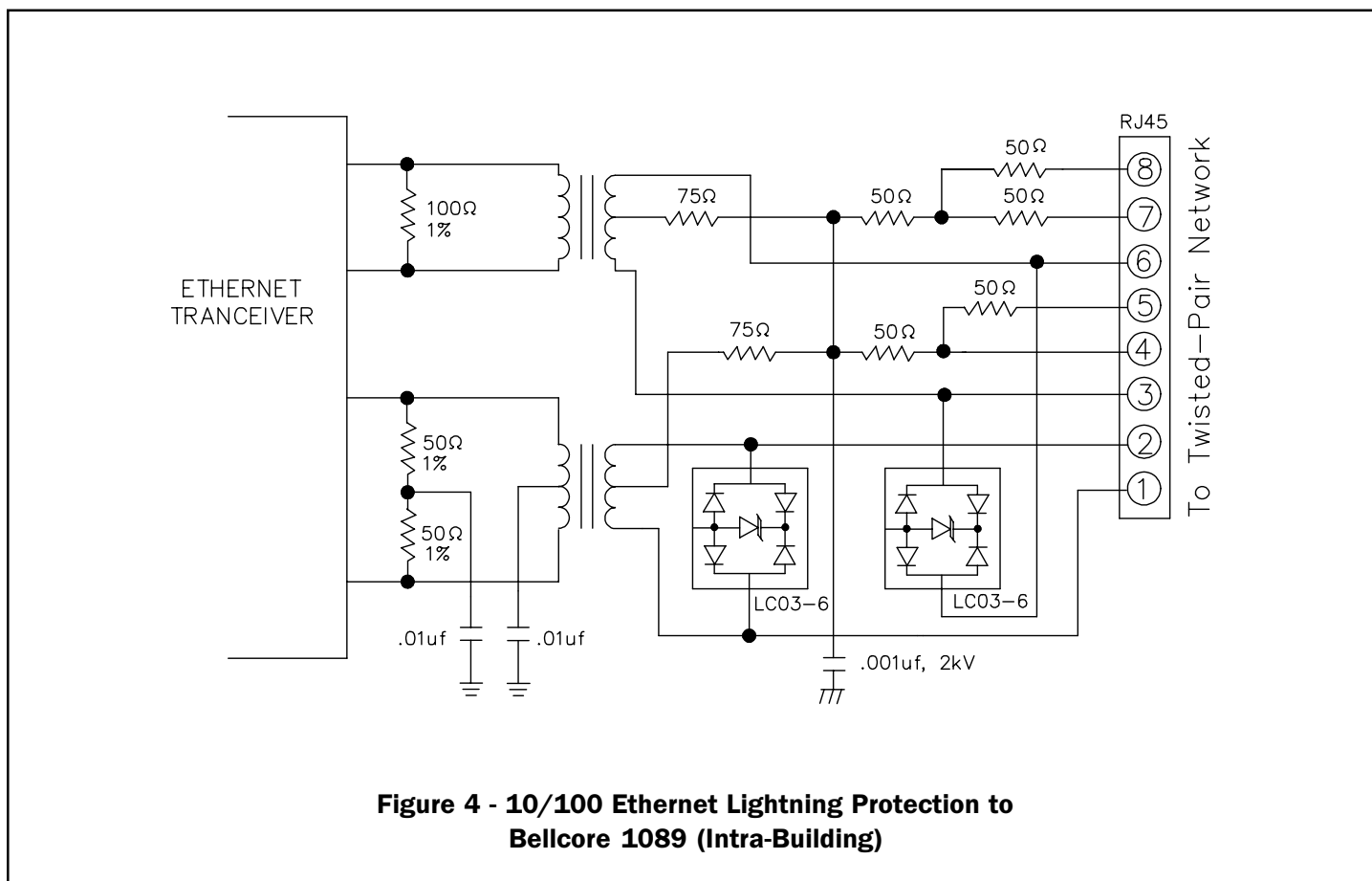


Figure 4 - 10/100 Ethernet Lightning Protection to Bellcore 1089 (Intra-Building)