APPLICATION NOTE

AN177

An overview of the phase-locked loop (PLL)

1988 Dec

Philips
Semiconductors

PHILIPS

An overview of the phase-locked loop (PLL) AN177

Portions of this Phase-Locked Loop section were edited by Dr. J. A. Connelly

INTRODUCTION

The basic phase-locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922. Since that time, PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems involved in these applications frequently are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been at microwave frequencies and employ complex phase shifters, signal splitters, modulation, and demodulation schemes such as bi-phase and quadra-phase. Because of the high frequencies involved in microwave applications, most all components of these PLL systems are made from discrete as opposed to integrated circuits. However, in other communication system applications such as FSK and FM and AM demodulation where frequencies are below approximately 100MHz, monolithic PLLs have found wide application because of their low cost versus high performance.

A block diagram representation of a PLL is shown in Figure 1. Phase-locked loops operate by producing an oscillator frequency to match the frequency of an input signal, fl. In this locked condition, any slight change in fl first appears as a change in phase between fl and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match fl. The locking onto a phase relationship between fl and the local oscillator accounts for the name phase-locked loop.

A MECHANICAL ANALOG TO THE PLL

To better visualize the frequency and phase relationships in a PLL, consider the mechanical system shown in Figure 2 which is a dual to the electronic PLL. This mechanical system has two identical, heavy disks with two separate center shafts attached to each disk. Each shaft is presumed to be mounted on a bearing that allows each massive disk to be rotated in either direction when some external force is applied. The shafts are coupled together by a spring whose end points are fixed to each shaft. This spring can be twisted in either direction, depending upon the relative positions of the shafts. The spring cannot ”kink up” due to the shafts passing through the center of the spring.

Now suppose the sequence of events shown in Figure 3 occurs to the mechanical system. The disks are simply represented like clock faces with positional reference markers. Initially, both disks are stationary in a neutral position. Then the left disk, or input, is advanced slowly clockwise through an angle ~~ position. The right disk, or output, initially doesn't move as the spring begins to tighten. As the input continues to move and when it reaches ~2. begins to turn and tracks the input with a positional phase shift error of ~e = ~2 (l)

At any point in time, with both disks slowly turning at the same speed, there will be some inherent phase error between the disks, or ~e = ~3 ~4 (2)

This positional phase error in the mechanical system is analogous to the phase error in the electronic PLL. When the input disk coasts to a stop, the output also gradually comes to a stop with a fixed phase error equal to that in Equation 2 or ~e = ~s ~6 = ~3 ~4 (3)

The spring has a residual stored twist in one direction due to ~e

Now consider that the disks are first returned to their neutral positions. Then the input disk is instantaneously rotated through an angle of ~l as shown in Figure 4. The output disk can't respond instantaneously because of its large mass. It doesn't move instantaneously and the spring develops considerable torque. Then, as shown in the sequence of events in Figure 4, the output disk begins accelerating after some delay due to the large phase error. It swings past the stopped position of the input disk due to its momentum, reaches a peak overshoot, and gradually oscillates about ~~ with a damped response, finally coming to rest with some small residual phase error. The input twist of ~1 represents the application of a step of position or phase to the system, and the response of the output disk is typical for a second-order, underdamped system. This same type of secondorder behavior occurs in the PLL system for an instantaneous change of input phase.

As a final example, consider the events in Figure 5 where both disks are rotating at a constant rate. Applying a strobing light (strobotac) simultaneously to both disks and adjusting its flashing rate to one flash per disk rotation will cause the positional markers to appear stationary. There will be a constant phase error in this case just as there was in Figure 3. Now suppose the revolution rate of the input disk gradually increases by a small amount to a new rate. The positional marker will appear to walk around the disk. The output first senses the increased rate of the input through an increase in the phase error.

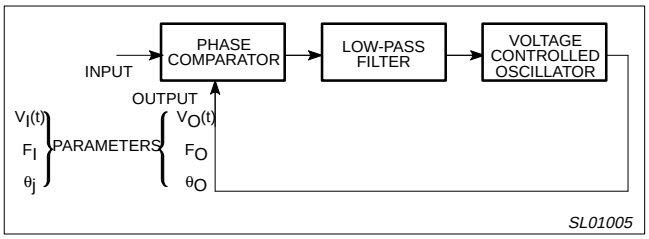

Figure 1. Block Diagram of a Phase-Locked Loop

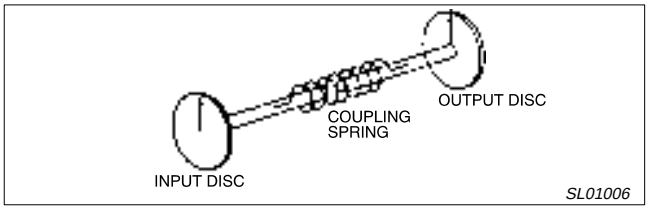

Figure 2. Mechanic Analog to PLL

Then, after some delay, the rate of the output gradually increases to track the input. Both positional markers appear to be walking around each disk at the same rate until the strobotac is adjusted for the higher input and output rate. Then the strobe light again freezes the markers, producing a phase error at this higher rate that is larger than before the input rate was increased. This gradual increase in the input rate to the mechanical system simulates a ramp change in the input frequency to the PLL system. The response to the output disk simulates the behavior of the oscillator in the PLL.

If the rate of the input disk is alternately increased and decreased by some small amount compared to the nominal revolution rate, the positional markers will appear to walk both clockwise and counter clockwise, momentarily appearing stationary when the strobing light rate equals the disk revolution rate. This ”walking” represents a changing phase error which is occurring at the modulation rate. Thus the phase error can be thought of as a useable demodulated output signal.

The disk-spring mechanical system is a helpful analog for visualizing frequency, phase, transient, and steady-state responses in the electronic phase-locked loop system. In this example, the positions

of the disk marker and rotation rates are analogous to phase and frequency in the electronic PLL system. The spring acts as a phase comparator to constantly sense the relative positions or phases of the disks. The torque developed in this spring acts as the driving force or input signal to turn the second disk.

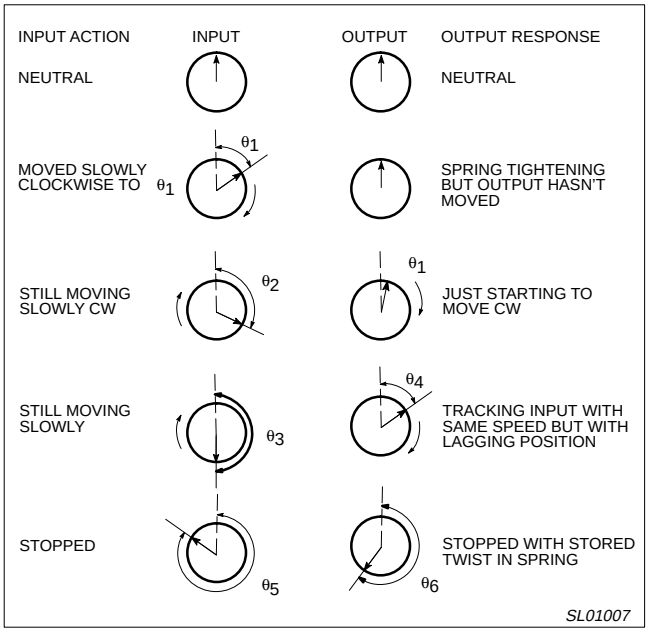

Figure 3. Disk Sequence Showing Output Tracking Input With Phase Error

Thus the spring torque simulates a voltage which controls the rate or frequency of the output disk or oscillator. Hence the second disk is analogous to a voltage-controlled oscillator (VCO). The large mass of the disks together with their angular momentum slows down the systems response time and simulates a low-pass filter in the electronic PLL system. This describes the lagging of the VCO free-running frequency to the input signal in an analog phase-locked loop.

EXAMPLES OF PLL APPLICATIONS

Now consider the action of the voltagecontrolled oscillator, phase comparator and low pass filter in the PLL. The VCO generates a signal that is periodic. Normally, the rate or frequency of the VCO is primarily determined by the value of a capacitance connected to this oscillator. This action of starting the VCO running by itself is analogous to disconnecting the spring from one of the shafts in the mechanical system and starting the output disk rotating at a constant rate through some external means such as a motor. In the PLL system this frequency is called the oscillator's free running frequency, (f_O'), because it occurs when the system is unlocked and there is no coupling between input and output frequencies. With the PLL, the VCO frequency can be shifted above and below f_O' by applying a voltage to the optional fine tune input.This signal generator property is just one of the many uses of the PLL. Specifically with integrated circuit PLLs, frequency ranges from less than 1.0Hz to more than 50MHz can be produced just by selecting the right value of capacitance from a chart on the data sheet.

Selecting f_O' and then changing it by a control voltage makes the VCO well suited for converting digital data that is represented by two different voltage levels into two different frequencies. A "l" voltage level can be related to a frequency called a mark, and an "0" level to a frequency called a space. This technique, called frequency shift keying, or (FSK), is typical of data being transmitted over telephone and radio links where it is impractical to use DC voltage level shifts. Essentially this is what a modem (modulator-demodulator) does as it converts data to tones to 90 out of the system into a transmission link. Then it reverses the process and converts received tones to "1"s and "0"s at the receiver for the system to use. Sometimes confusion arises because different names are used for the same thing. For example,

A shift up in frequency = "1" = Mark

A shift down in frequency = "0" = Space

NOTE: Some oscillators have frequencies controlled by an input current rather than a voltage and are retoned to as current-controlled oscillators (CCO).

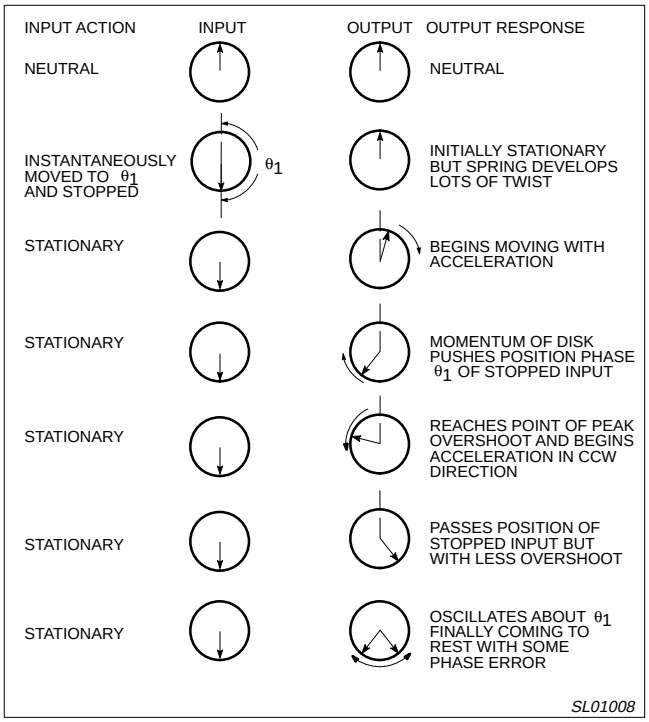

Figure 4. Disk Sequence Showing Output Response to a Sudden Position Input

If voice or music is applied to the VCO instead of digital data, the oscillator's frequency will move or modulate with the voice or music. This is frequency modulation (FM) and is simply moving the frequency in relation to some input voltage which represents intelligence. Of course, as in the modem case, the process has to be reversed and the PLL can do this also. The PLL is a complete working system that can be used to send and receive signals. In fact the PLL can create the signal, or select a signal, decode it and reproduce it. Now let's look at how this works.

The VCO is connected to a section where its frequency is put together with an incoming signal or signals. In a radio this is known as a "mixer" where signals are mixed together. In a PLL it is usually called a Phase Comparator Other names for this function are phase detector or multiplier — either analog or digital. (Differences between analog and digital phase comparators will be explained later in this chapter.) The purpose of this phase comparator is to produce an output which represents how far the VCO frequency is

from that of the incoming signal. Comparing these frequencies and producing an error signal proportional to their difference allows the VCO frequency to shift from f_O' and become the same frequency as the input signal. This is exactly what happens with the VCO frequency — first "capturing" the input frequency, and then locking onto it. A similar type of action can be visualized in the mechanical system by having the coupling spring disconnected at one end with the two disks rotating at different rates. When their rotation rates are approximately equal, the spring is suddenly connected, and the output disk's speed will gradually become equal to and track the inputs rate as in Figure S.

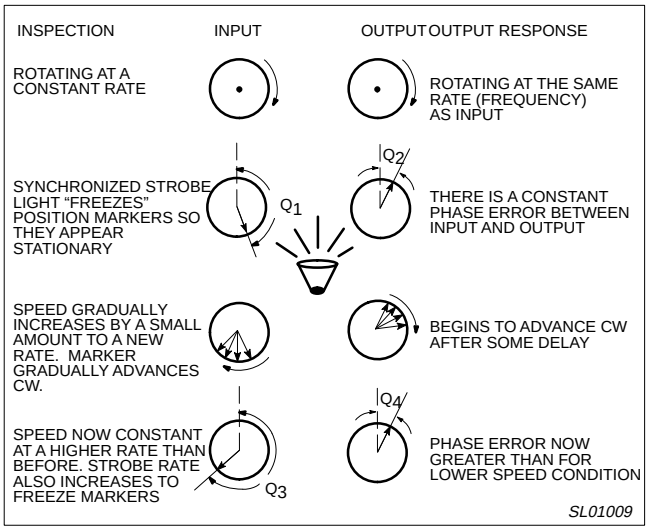

Figure 5. Disk Sequence Showing Output Behavior Due to Changes In Input Speed

When the VCO shifts frequency and locks to the input, the signal frequency is duplicated. If the input signal contains static or noise, the VCO output will be an exact reproduction of the signal frequency without the static or noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

The error signal used to keep the VCO exactly synchronized with an incoming signal can be amplified, filtered, and used to "clock" the signal or give synchronizing information necessary to look at the signal. For example, in some digital memories and transmission systems, data are stored in a code and looked at or strobed at a rate which must be synchronized to the data. This strobing may be at twice or one-half the data rate. By setting f_O' equal to twice or one-half the data rate, the PLL will lock to the data and give an exact synchronized clock. This shows another application of the PLL for multiplying or dividing frequencies.

PLLs can separate a signal of one frequency from among many others as, for example, is done in television and radio reception. This 1 selectivity or capture range is controlled in 2 the PLL by the low-pass filter (LPF) which 3 allows the PLL to only see signals close to the frequency of interest. The time constant 4 of the LPF is set easily by the selection of a S. resistor and capacitor network. This network determines how far away in frequency an 6 input signal can be from f_O' and still permit the PLL to respond and capture. Once locking is activated, the PLL system will continue to track the input frequency unless the instantaneous phase error exceeds the system's capability.

The error signal which drives the VCO and keeps the system locked is a usable output. In the FSK example the oscillator's frequency is shifted with each "l" or "O" digital input. Converting these frequency shifts back to the "l" and "O" signals automatically occurs in a PLL because a mark input generates an error signal to move the VCO up to that frequency. When the mark changes to a space, the error signal jumps suddenly down, forcing the VCO to follow. The error signal then is exactly the data that generated the FSK signals. A PLL for fSK can convert data to tones for transmission to a remote point. Then another PLL can reconvert the data tones back to voltage levels, all without tuned circuits.

The PLL system decodes FM signals in a similar way. The frequency variations caused by voltages from a microphone into one VCO serve as the input signal to another PLL, which reverses the action since the error signal driving the second PLL's VCO is exactly the same as the original microphone voltage.

Decoding of an amplitude-modulated (AM) input signal is another application of the PLL. This application is more involved than FM demodulation because a phase shift network, a second-phase comparator, and another low-pass filter are required. This application is discussed in detail later. However, it should be pointed out that AM demodulation with PLLs offers improved system linearity than the more commonly employed technique of nonlinear diode detection. Tone decoding is a special case of AM demodulation. When performed with PLLs, the second-phase comparator is called a quadrature-phase detector (—PD). The —PD produces a maximum output error voltage whenever the input and oscillator frequencies are locked to the free-running frequency, f_O', unlike the regular phase comparator which has a nominal zero error voltage under this same condition.

These application examples show that with the PLL, a system can: Generate a signal ~. Modulate a signal (encode)

Select a signal from among many, Demodulate (decode) Recreate (reconstitute) a signal frequency with reduced noise Multiply and divide frequency.

TYPES OF PLLS

Generally speaking, the monolithic PLLs can be classified into two groups — digital and analog. While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

The phase comparator is perhaps the most important part of the PLL system since it is here that the input and VCO frequencies are simultaneously compared. Some digital PLLs employ a two-input Exclusive-OR gate as the phase comparator. When the digital loop is locked to f_O', there is an inherent phase error of 90! that is represented by asymmetry in the output waveform. Also, the phase comparator's output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase comparators achieve locking by synchronizing the "edges" of the input and VCO frequency waveshapes. The phase comparator produces an error voltage that is proportional to the time difference between the edges; i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the ExclusiveOR approach. However, time line, on the input and VCO frequencies is translated into phase error line, that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle. This is a key

consideration in PLL applications utilizing counters where waveshapes usually aren't symmetrical; i.e., 50% duty cycle. For the TTL family, it is easier to provide the edge matching function on the falling edges ("l" to "O") transition of the waveform. CMOS, 12L, and ECL are better suited for leading edge triggering ("O" to "1").

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals. Since this mixing is true analog multiplication, the phase comparator's output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications.

Another way of distinguishing between digital and analog phase comparators is by thinking of the similarities and differences between voltage comparators and operational amplifiers. Voltage comparators are specially designed for digital applications where response time between output levels has been minimized at the expense of system linearity. Feedback is seldom used to maintain linear system relationships, with the comparator normally running open-loop. Op amps, on the other hand, are designed for a linear inputoutput relationship, with negative feedback being employed to further improve the system linearity.

PLL TERMINOLOGY

The following is a brief glossary of frequently encountered terms in PLL literature.

Free-running Frequency (f_O', ω_O') — Also called the center frequency, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_O and ω_O which are used for the general oscillator frequency. (Many references use f_O and ω_O for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context.) The appropriate units for f_O' and ω_O' are Hz and radians per second, respectively.

Lock Range ($2f_L$, $2\omega_L$)* — The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency, unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_O'. The deviations from f_O' are referred to as the *Tracking Range or Hold-in Range*. (See Figure 6). The tracking range is therefore one-half of the lock range.

Capture Range ($2f_C$, $2\omega_C$)** — Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_O' with the equal deviations called the *Lock-in* or *Pull-in Ranges. The capture range can never exceed the lock range.*

Lock-up Time (t_L)*** — The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the lowpass filter. *The lock-up time is inversely proportional to the selectivity bandwidth.* Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Phase Comparator Conversion Gain (K_d) — The conversion constant relating the phase comparator's output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/ rad).

VCO Conversion Gain (K_O) — The conversion constant relating the oscillator's frequency shift from f_O' to the applied input voltage. K_O has units of radians per second per volt (rad/sec/V). K_O is a linear function of ω_O' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_O'.

Loop Gain (K_V) — The product of K_d, K_O, and the low-pass filters gain at DC. K_d is evaluated at the appropriate input signal level and K_O at the appropriate ω_O'. K_V has units of $(sec)^{-1}$.

Closed-Loop Gain (CLG) — The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_V}{1 + K_V} \quad (4)$$

Natural Frequency (ω_n) — The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_O' and at which the phase error swing is the greatest.

Damping Factor (ζ) — The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Loop Noise Bandwidth (B_L) — A loop property relating ω_n and ζ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

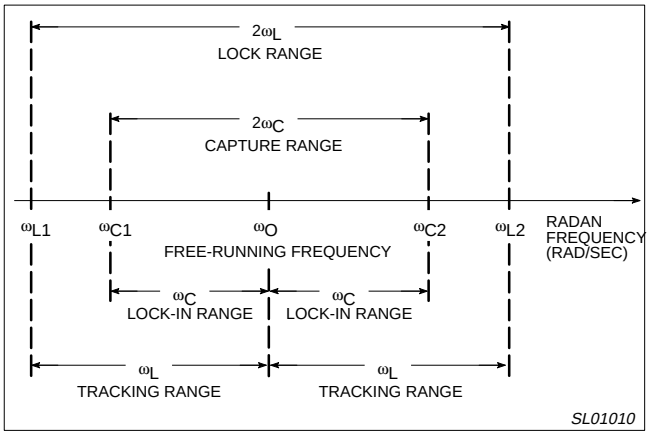

Figure 6. Lock and Capture Range Relationships

REFERENCES

1. Appleton, E.V., "Automatic Synchronization of Triode Oscillators", *Proc. Cambridge Phil. Soc.*, vol. 2, pt. Ill, p.231, 1922 –1923.
2. Gardner, F.M., *Phaselock Techniques*, New York: Wiley, 1966.
3. Blanchard, A., *Phase-Locked Loops*, New York: Wiley, 1976.
4. Viterbi, A.J., *Principles of Coherent Communications*, New York: McGraw-Hill, 1966.
5. Connelly, J.A., *Analog Integrated Circuits: Devices, Circuits, Systems, and Applications*, New York: Wiley, 1975.

6. Grebene, A.B., *Analog Integrated Circuit Design*, New York: Van Nostrand-Reinhold, 1972.

7. Staff, *Philips Semiconductors Linear Phase Locked Loops Applications Book*, Philips Semiconductors Corporation, Sunnyvale. California. 1972.

8. Gupta, s.c., "Phase-Locked Loops," *Proc. IEEE*, vol. 63, no. 2, pp. 291–306, Feb. 1975.

9. D'Azzo, J.J. and C.H. Houpis, *Feedback Control System Analysis* (Second Edition), New York: McGraw-Hill, 1966, p.81.

10. Gilbert, B., "A New Wideband Amplifier Technique," *IEEE J. of Solid State Ckts.*, SC-3(4), pp. 353-365, 1968.

11. Gardner, op. cit., pp. 117-119.

12. Milligan, L.V. and E. Cornicelli, "Phase Locked Loops Provide Accurate, Efficient DC Motor Speed Control," *EDN*, August 1, 1972, pp. 32-35.

13. Dr. Roland E. Best, *Phase Locked Loops — Theory, Design & Applications*, McGraw-Hill.

NOTES:

*Also called Synchronization Range.

**Also called Acquisition Range.

***Also called Acquisition Time.