

## SELF-OSCILLATING HALF-BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Undervoltage lockout
- Programmable oscillator frequency

$$f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$$

- Matched propagation delay for both channels
- Low side output in phase with R<sub>T</sub>

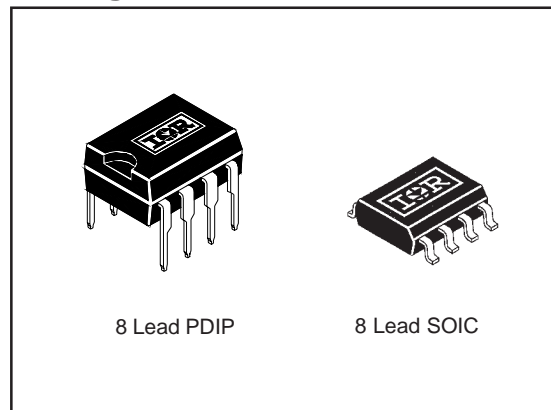
### Description

The IR2152 is a high voltage, high speed, self-oscillating power MOSFET and IGBT driver with both high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal deadtime designed for minimum driver cross-conduction. Propagation delays for the two channels are matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration that operates off a high voltage rail up to 600 volts.

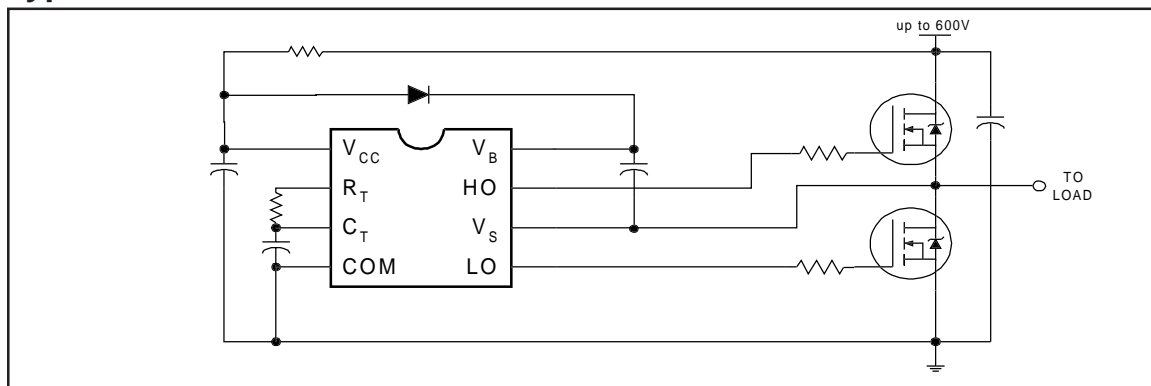
### Product Summary

V <sub>OFFSET</sub>	600V max.
Duty Cycle	50%
I <sub>O+/-</sub>	100 mA / 210 mA
V <sub>OUT</sub>	10 - 20V
Deadtime (typ.)	1.2 μs

### Packages



### Typical Connection



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply voltage	-0.3	625	V
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>RT</sub>	R <sub>T</sub> voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>CT</sub>	C <sub>T</sub> voltage	-0.3	V <sub>CC</sub> + 0.3	
I <sub>CC</sub>	Supply current (note 1)	—	25	mA
I <sub>RT</sub>	R <sub>T</sub> output current	-5	5	
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R <sub>THJA</sub>	Thermal resistance, junction to ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High Side Floating Supply Absolute Voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	—	600	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>LO</sub>	Low Side Output Voltage	0	V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current (Note 1)	—	5	mA
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Note 1: Because of the IR2152's application specificity toward off-line supply systems, this IC contains a zener clamp structure between the chip V<sub>CC</sub> and COM which has a nominal breakdown voltage of 15.6V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip V<sub>CC</sub> and the rectified line voltage and a local decoupling capacitor from V<sub>CC</sub> to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than V<sub>CLAMP</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_r$	Turn-on rise time	—	80	120	ns	
$t_f$	Turn-off fall time	—	40	70		
DT	Deadtime	0.50	1.20	2.25	μs	
D	$R_T$ duty cycle	48	50	52	%	

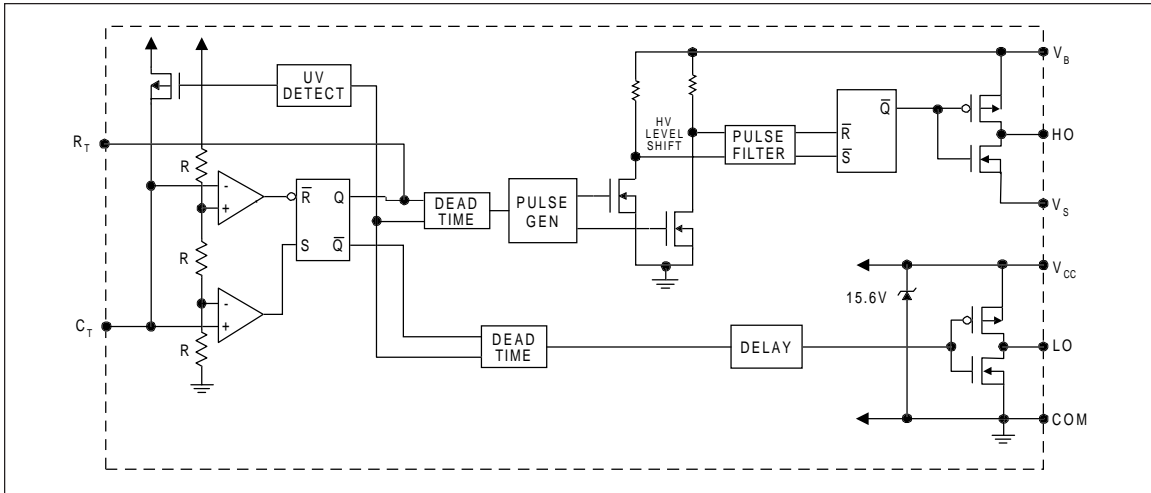
## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12V,  $C_L$  = 1000 pF,  $C_T$  = 1 nF and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$f_{OSC}$	Oscillator frequency	19.4	20.0	20.6	kHz	$R_T = 35.7 \text{ k}\Omega$
		94	100	106		$R_T = 7.04 \text{ k}\Omega$
$V_{CLAMP}$	$V_{CC}$ zener shunt clamp voltage	14.4	15.6	16.8	V	$I_{CC} = 5 \text{ mA}$
$V_{CT+}$	2/3 $V_{CC}$ threshold	7.8	8.0	8.2		
$V_{CT-}$	1/3 $V_{CC}$ threshold	3.8	4.0	4.2	mV	$2.5V < V_{CC} < V_{CCUV+}$
$V_{CTUV}$	$C_T$ undervoltage lockout, $V_{CC} - C_T$	—	20	50		$I_{RT} = -100 \mu\text{A}$
$V_{RT+}$	$R_T$ high level output voltage, $V_{CC} - R_T$	—	0	100		$I_{RT} = -1 \text{ mA}$
		—	200	300		$I_{RT} = 100 \mu\text{A}$
$V_{RT-}$	$R_T$ low level output voltage	—	20	50		$I_{RT} = 1 \text{ mA}$
		—	200	300		$2.5V < V_{CC} < V_{CCUV+}$
$V_{RTUV}$	$R_T$ undervoltage lockout	—	0	100		$I_O = 0 \text{ A}$
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	100		$I_O = 0 \text{ A}$
$V_{OL}$	Low level output voltage, $V_O$	—	—	100	$V_B = V_S = 600 \text{ V}$	
$I_{LK}$	Offset supply leakage current	—	—	50	μA	
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	10	50		
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	400	950		
$I_{CT}$	$C_T$ input current	—	0.001	1.0	V	
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	7.7	8.4	9.2		
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.1	8.9		
$V_{CCUVH}$	$V_{CC}$ supply undervoltage lockout hysteresis	200	500	—	mV	
$I_{O+}$	Output high short circuit pulsed current	100	125	—	mA	$V_O = 0 \text{ V}$
$I_{O-}$	Output low short circuit pulsed current	210	250	—		$V_O = 15 \text{ V}$

# IR2152

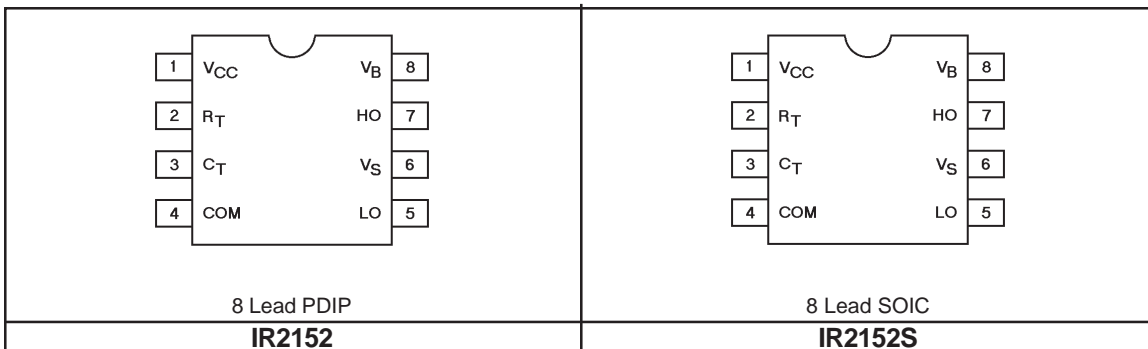
## Functional Block Diagram

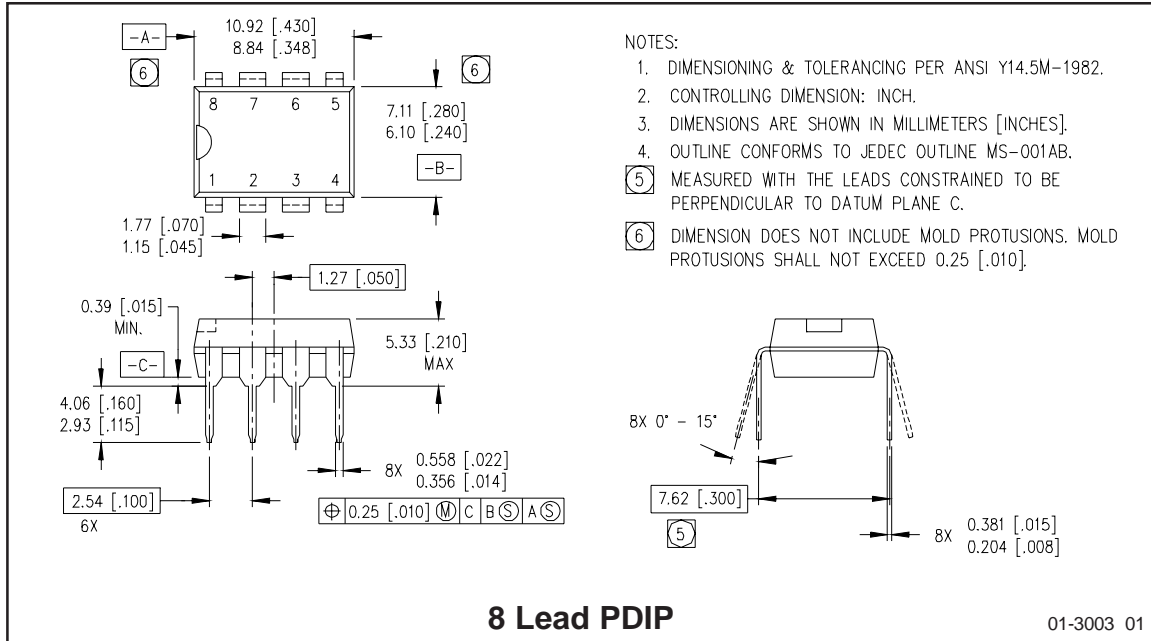


### Lead Definitions

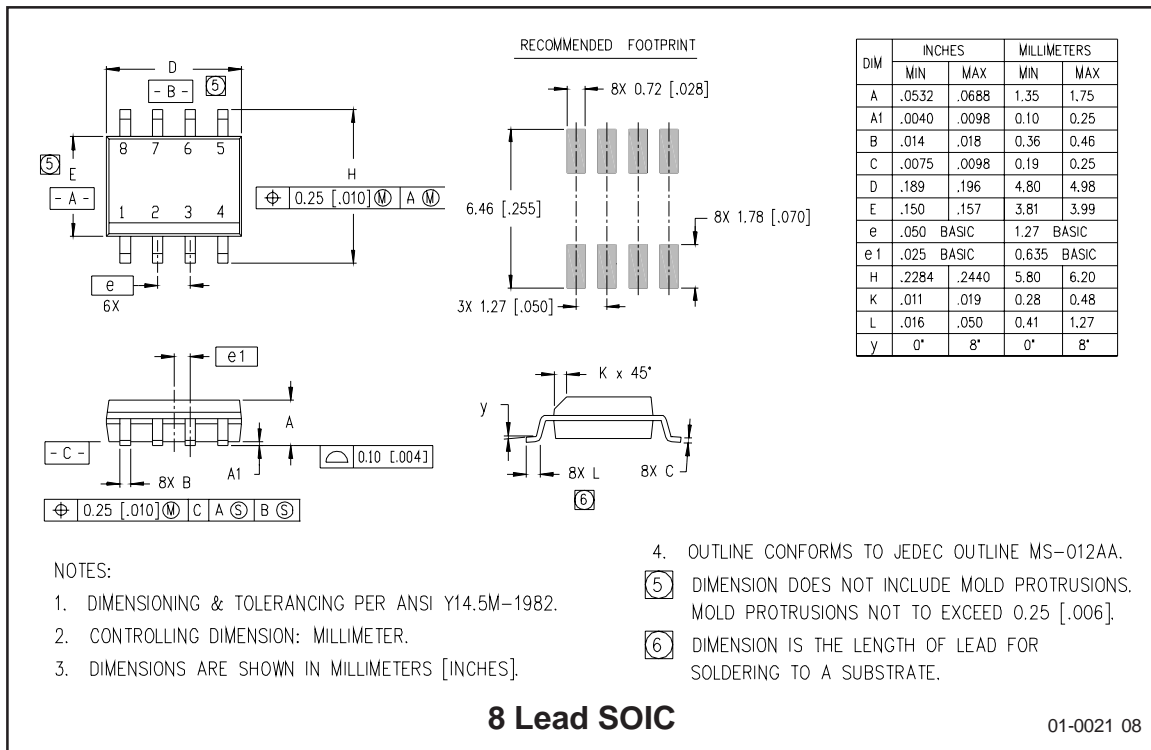
Symbol	Description
R <sub>T</sub>	Oscillator timing resistor input, in phase with HO for normal IC operation
C <sub>T</sub>	Oscillator timing capacitor input, the oscillator frequency according to the following equation: $f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$ where 75Ω is the effective impedance of the R <sub>T</sub> output stage
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

### Lead Assignments





- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
  - 5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
  - 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050	BASIC	1.27	BASIC
e1	.025	BASIC	0.635	BASIC
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
  - 5 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.25 [.006].
  - 6 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

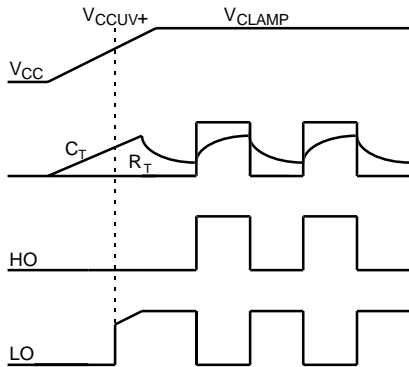


Figure 1. Input/Output Timing Diagram

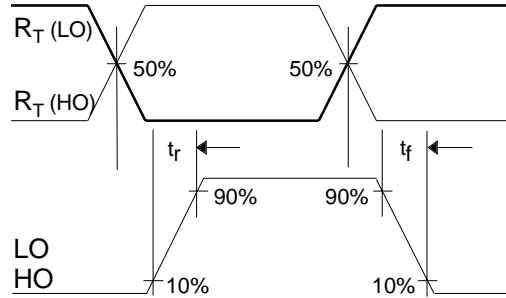


Figure 2. Switching Time Waveform Definitions

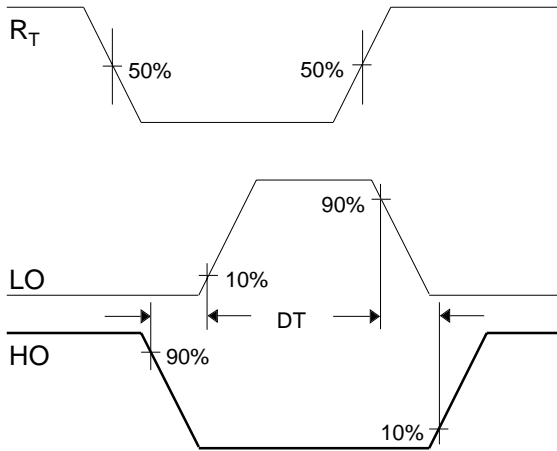


Figure 3. Deadtime Waveform Definitions