HM67S18258 Series

4M Synchronous Fast Static RAM (256k-words × 18-bits)

HITACHI

ADE-203-661B(Z)
Product Preview, Rev. 2
Nov. 18, 1997

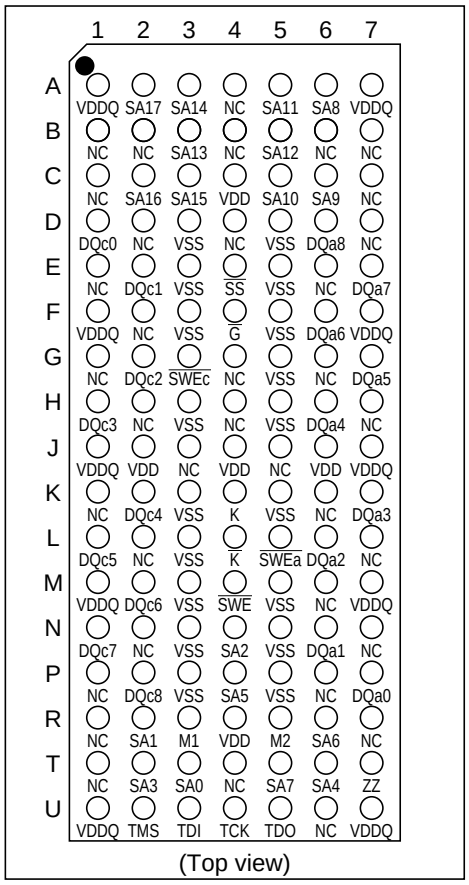
Features

- 3.3V ± 5% Operation
- LVCMOS Compatible Input and Output
- Synchronous Operation
- Internal self-timed Late Write
- Asynchronous $\overline{G}$ Output Control
- Byte Write Control
  (2 byte write selects, one for each 9 bits)
- Power down mode is provided
- Differential PECL Clock Inputs
- Boundary Scan
- Protocol Single Clock Resister-Latch Mode

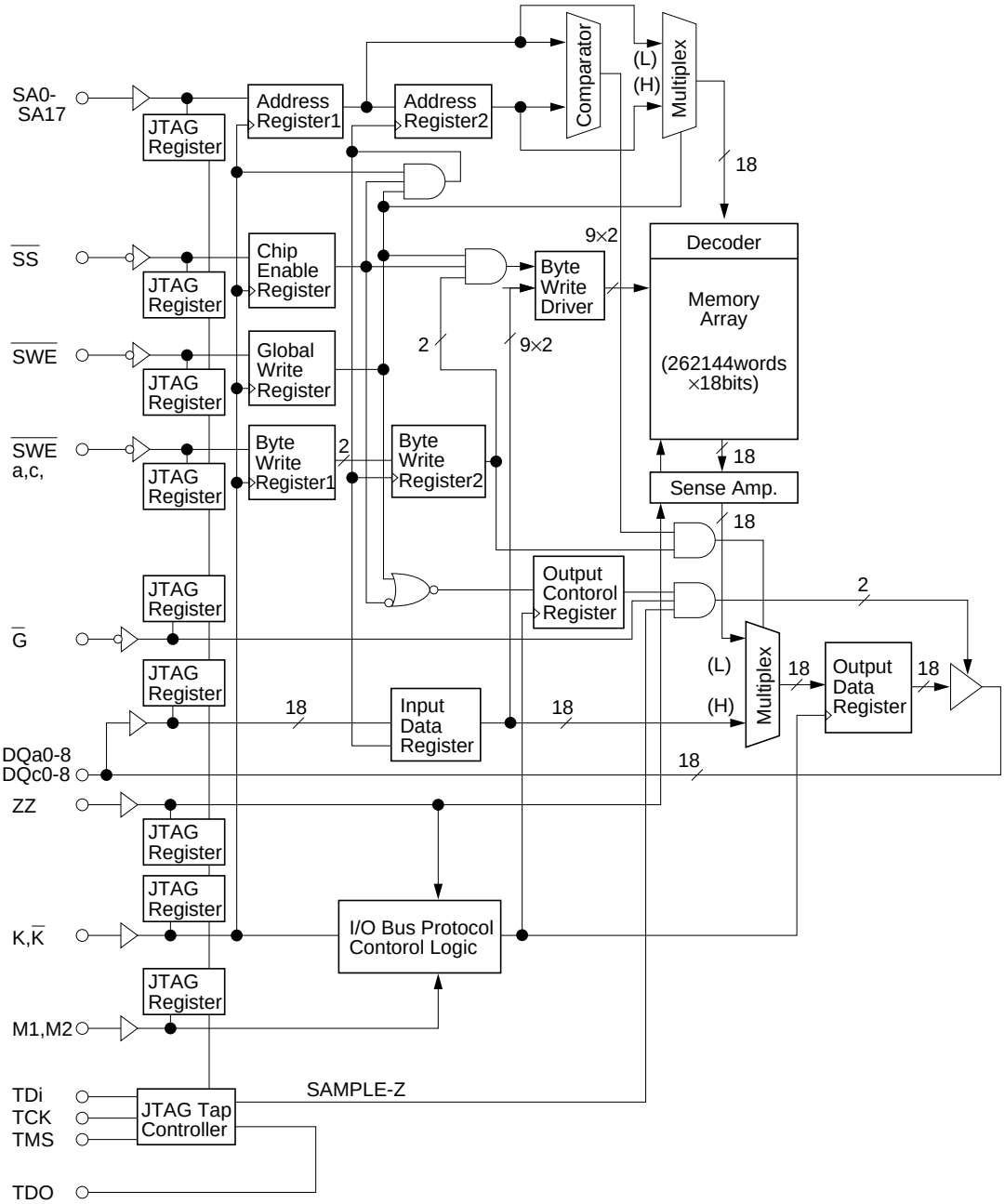
Ordering Information

Type Number	Cycle Time	Package
HM67S18258BP-7	7.0 ns	119 Bump 1. 27 mm 14 mm × 22 mm BGA (BP-119A)

Pin Arrangement



Block Diagram



Note: The functional block diagram illustrates simplified device operation. See truth table, pin descriptions and timing diagrams for detailed information.

Pin Descriptions

Name	I/O Type	Descriptions	Note
V_{DD}		Power Supply	
V_{SS}		Ground	
V_{DDQ}		Output Power Supply	
K	Input	Input Clock	
$\overline{K}$	Input	Input Clock	
$\overline{SS}$	Input	Synchronous Chip Select	
$\overline{SWE}$	Input	Synchronous Write Enable	
SAn	Input	Synchronous Address	n = 0, 1, 2, ... 17
$\overline{SWEx}$	Input	Synchronous Byte Select	x = a, c
$\overline{G}$	Input	Asynchronous Output Enables	
ZZ	Input	Power Down Mode Select	
DQxm	I/O	Synchronous Data Input/Output	x = a, c m = 0, 1, 2, ... 8
M1, M2	Input	Output Protocol Mode Select	1
TMS	Input	Boundary Scan Test Mode Select	
TCK	Input	Boundary Scan Test Clock	
TDI	Input	Boundary Scan Test Data In	
TDO	Output	Boundary Scan Test Data Out	
NC		No Connection	

Notes: 1. There is 1 protocol with using mode pins. Mode control pins (M1, M2) are to be tied to either V_{DD} or V_{SS}. The state of the Mode control inputs must be set before power-up and must not change during device operation. Mode control inputs are not standard inputs and may not meet V_{IH} or V_{IL} specifications.

M1	M2	Protocol
V_{DD}	V_{SS}	Single Clock Register Latch

Truth Table

$\overline{SS}$	$\overline{G}$	$\overline{SWE}$	$\overline{SWEa}$	$\overline{SWEc}$	K	$\overline{K}$	Operation	DQa	DQc
H	X	X	X	X	L-H	H-L	Dead (not selected)	High-Z	High-Z
L	H	H	X	X	L-H	H-L	Dead (Dummy read)	High-Z	High-Z
L	L	H	X	X	L-H	H-L	Read	Dout	Dout
L	X	L	L	L	L-H	H-L	Write	Din	Din
L	X	L	H	L	L-H	H-L	Write	High-Z	Din
L	X	L	L	H	L-H	H-L	Write	Din	High-Z

Notes: 1. X means don't care for synchronous inputs, and H or L for asynchronous inputs.
2. $\overline{SWE}$, $\overline{SS}$, $\overline{SWEa}$, $\overline{SWEc}$, SA are sampled at the rising edge of K clock.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.5 to +4.6	V	1
Output Supply Voltage	V_{DDQ}	–0.5 to V_{DD}+0.5	V	1, 4
Voltage on any pin	V_{IN}	–0.5 to V_{DD}+0.5	V	1, 4
Operating Temperature	Ta	0 to 70 (Tj max = 110)	°C	
Storage Temperature	Tstg (bias)	–55 to 125	°C	
Input Latchup Current	I_{LI}	±200	mA	
Output Current per pin	Iout	±25	mA	

Notes: 1. All voltage are referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These Bi-CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. Not exceed 4.6 V
5. Power Up Initialization

The following supply voltage application sequence is recommended: V_{SS}, V_{DD} then V_{DDQ}.

Remember according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed V_{DD} + 0.5 V, whatever the instantaneous value of V_{DD}.

Recommended DC Operating Conditions (Ta = 0 to 70°C [Tj max = 110°C])

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	3.135	3.3	3.465	V	
Output Supply voltage	V_{DDQ}	3.135	3.3	3.465	V	1
		2.375	2.5	2.75	V	2
Input voltage Logic High Level	V_{IH}	2.0	—	V_{DDQ} + 0.3	V	1
Logic Low Level	V_{IL}	–0.5	—	0.8	V	1
Logic High Level	V_{IH}	1.85	—	V_{DDQ} + 0.3	V	2
Logic Low Level	V_{IL}	–0.5	—	1.15	V	2
PECL Logic High Level	V_{IH}(PECL)	2.135	—	2.420	V	
PECL Logic Low Level	V_{IL}(PECL)	1.490	—	1.825	V	

Note: 1. For V_{DDQ} = 3.3 V supply.
2. For V_{DDQ} = 2.5 V supply.

DC Characteristics (Ta = 0 to 70°C [Tj max 110°C], V_{DD} = 3.3V± 5%)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Input Leakage Current		I_{LI}	–1	—	1	µA	1
Output Leakage Current		I_{LO}	–1	—	1	µA	2
PECL Input Leakage Current Low		I_{LI} (PECL)		—	50	µA	
PECL Input Leakage Current High		I_{LI} (PECL)		—	150	µA	
V_{DD} Operating Current excluding output drivers		I_{DD}	—	—	600	mA	3
Power Dissipation including output drivers		P_d	—	—	2.7	W	3, 8
Standby Current (Power down mode)		I_{SB}	—	—	100	mA	5
Output Voltage	Logic Low	V_{OL}	0	—	0.4	V	4
	Logic High	V_{OH}	2.4 V_{DDQ}-0.4	—	V_{DDQ} V_{DDQ}	V V	4, 6 4, 7

Note: 1. $0 \le Vin \le V_{DD}$
2. $0 \le VI/O \le V_{DD}$, Tristate I/O
3. I(I/O) = 0 mA, Address increment read 50% / write 50%, $V_{DD} = V_{DD}$ max, Frequency = 125 MHz
4. I_{OH} = –2 mA or I_{OL} = 2 mA
5. All inputs (except clock) are held at either V_{SS} or V_{DDQ}, and ZZ is held at V_{DDQ}
6. for V_{DDQ} = 3.3 V supply
7. for V_{DDQ} = 2.5 V supply
8. Output Load Capacitance = 29 pF

Input Capacitance (Ta = 25°C, f = 1 MHz)

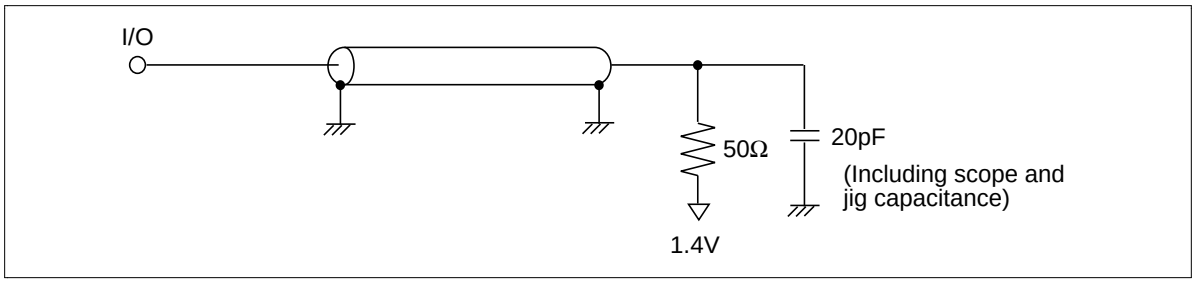
Parameter	Symbol	Min	Max	Unit	Pin Name	Note
Address Input Capacitance	C_{INA}	—	5	pF	SAn, $\overline{SS}$, $\overline{SWE}$, $\overline{SWEx}$	1
Clock Input Capacitance	C_{INC}	—	8	pF	K, $\overline{K}$, $\overline{G}$	1
I/O Capacitance	C_{INIO}	—	7	pF	DQxm	1

Note: 1. This value is measured by sampling and not 100% tested.

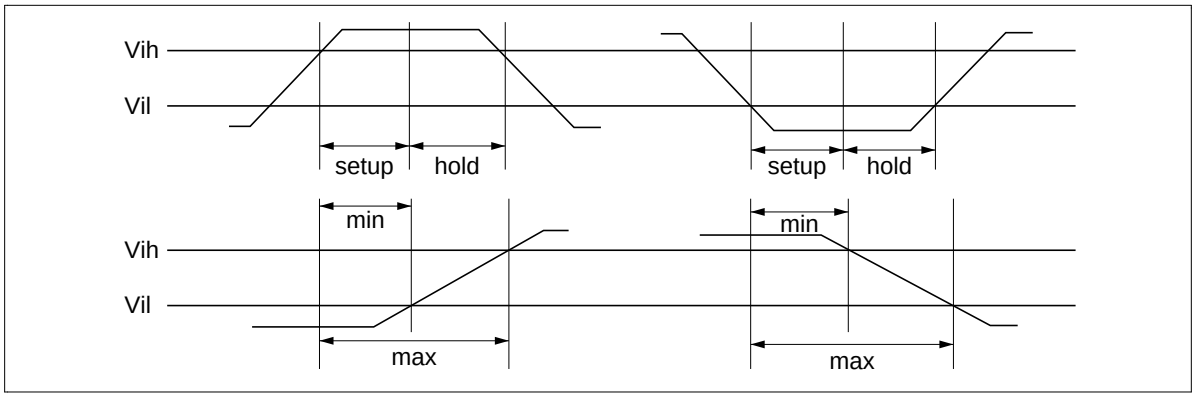
AC Test Conditions

		Note
• Temperature	0°C ≤ Ta ≤ 70°C (Tj max = 110°C)	
• Input Reference Point for Differential Signals	Differential Cross-Over Point	
• Input pulse levels	0 to 2.5 V	
• Clock Input pulse levels	1.8 to 2.1 V	
• Input Rise/Fall Time	0.5 to 1.5 ns (10% to 90%)	
• Clock input Rise/Fall Time	0.3 to 1.0 ns (10% to 90%)	
• Output timing reference (vih/vil)	2.0 V/0.8 V for V_{DDQ} = 3.3 V	1
	1.65 V/1.15 V for V_{DDQ} = 2.5 V	1
• Output load	See figures	

Note: 1. These levels are efficient under open termination load condition.
These vih/vil levels under termination load will be determined by correlation between open load and termination load.



AC Timing Measurement



AC Characteristics (Ta = 0° to 70°C [Tj max = 110°C], V_{DD}=3.3V± 5%)

Single Differential Clock Register-Latch Mode (M1 = V_{DD}, M2 = V_{SS})

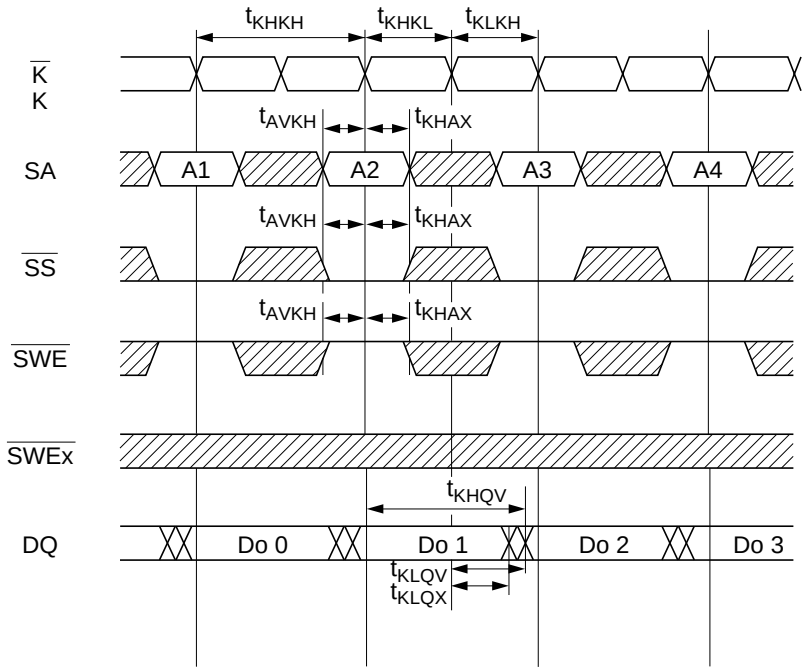
		-7			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Clock Control					
Clock Cycle	t_{KHKH}	8.0	—	ns	
Clock High Width	t_{KHKL}	2.0	—	ns	
Clock Low Width	t_{KLKH}	2.0	—	ns	
Read Control					
K Clock Access	t_{KHQV}	—	7.0	ns	
K Clock Access	t_{KLQV}	—	3.0	ns	
Output Enable Access	t_{GLQV}	—	3.5	ns	
K Low to Q Change	t_{KLQX}	1.0	—	ns	
Output Buffer Control					
K Low to Low-Z	t_{KLQX2}	1.0	—	ns	1
Output Enable to Low-Z	t_{GLQX}	1.0	—	ns	1
K Clock High to Hi-Z	t_{KHQZ}	1.0	3.5	ns	2
Output Enable to Hi-Z	t_{GHQZ}	0.0	3.5	ns	2
Setup Times					
Address Setup Time	t_{AVKH}	0.5	—	ns	SA, $\overline{SS}$, $\overline{SWE}$,
Data Setup Time	t_{DVKH}	0.5	—	ns	$\overline{SWEa}$, $\overline{SWEc}$
Hold Times					
Address Hold Time	t_{KHAX}	1.0	—	ns	SA, $\overline{SS}$, $\overline{SWE}$,
Data Hold Time	t_{KHDX}	1.0	—	ns	$\overline{SWEa}$, $\overline{SWEc}$

Notes: 1. Transition is measured ±200 mV from steady voltage with specified loading in Test Load.
2. Transition is measured start point of output high impedance from output Low impedance.

Timing Waveforms

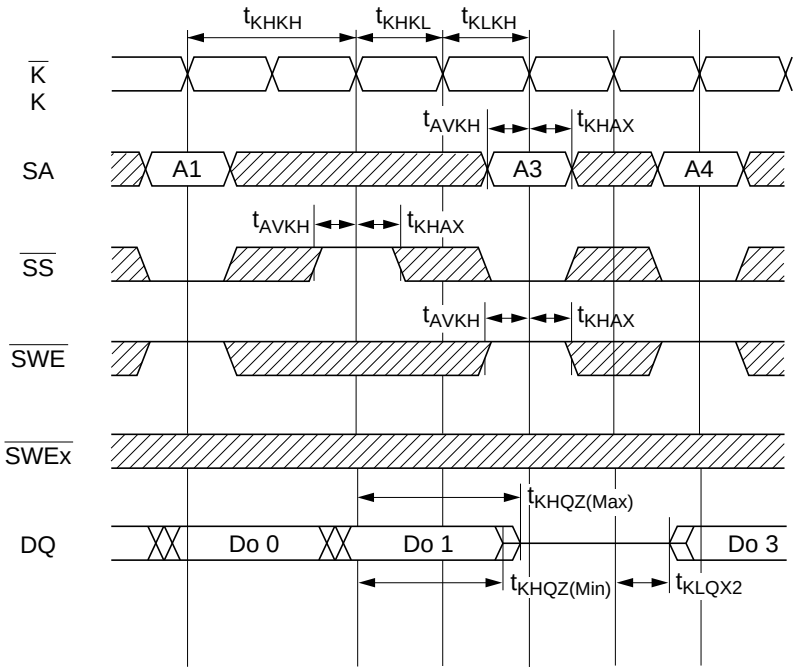
Single Clock Register Latch Mode

Read Cycle 1



Notes: $\overline{G} = V_{IL}$

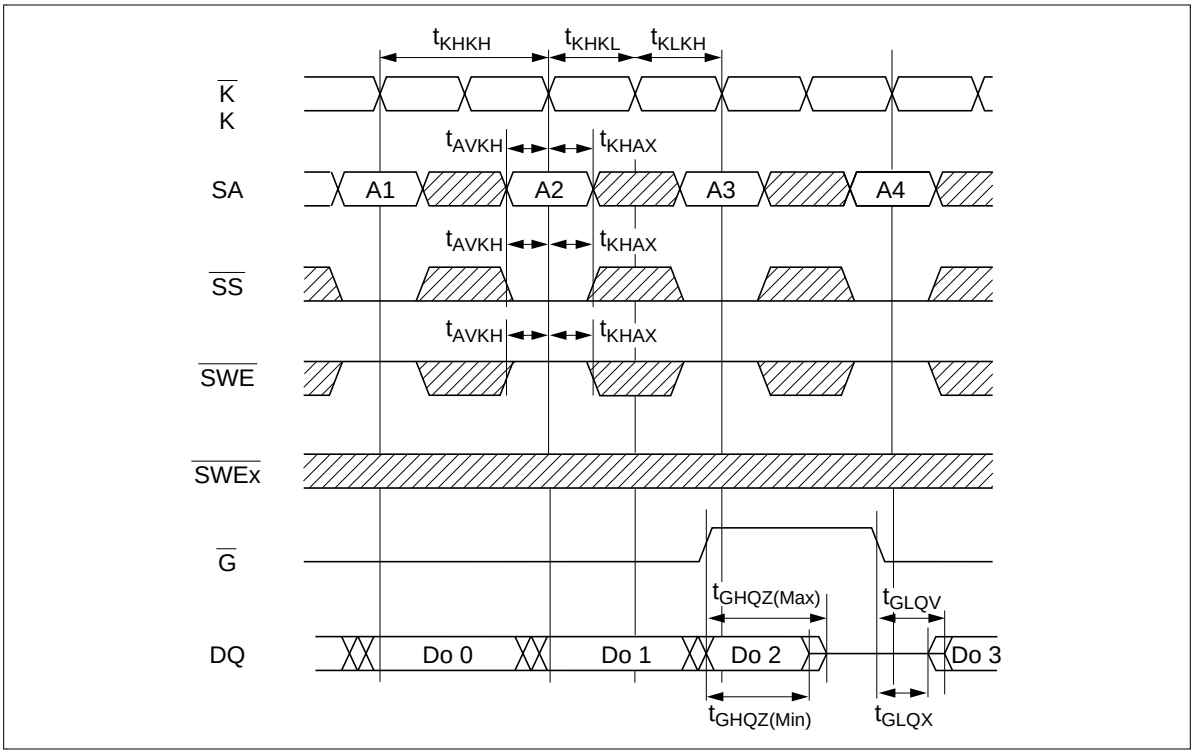
Read Cycle 2 ($\overline{SS}$ Controlled)



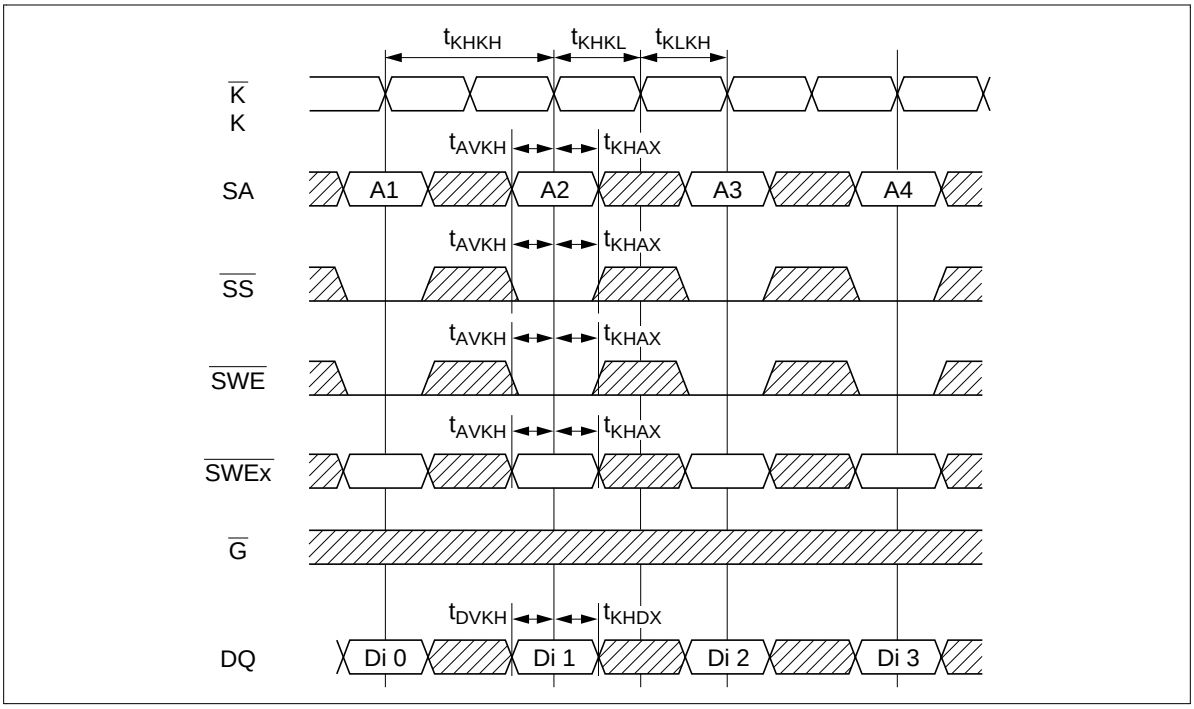
Note: 1. $\overline{G}$ =V_{IL}.

2. Do1 represents the output data for the input address A1.

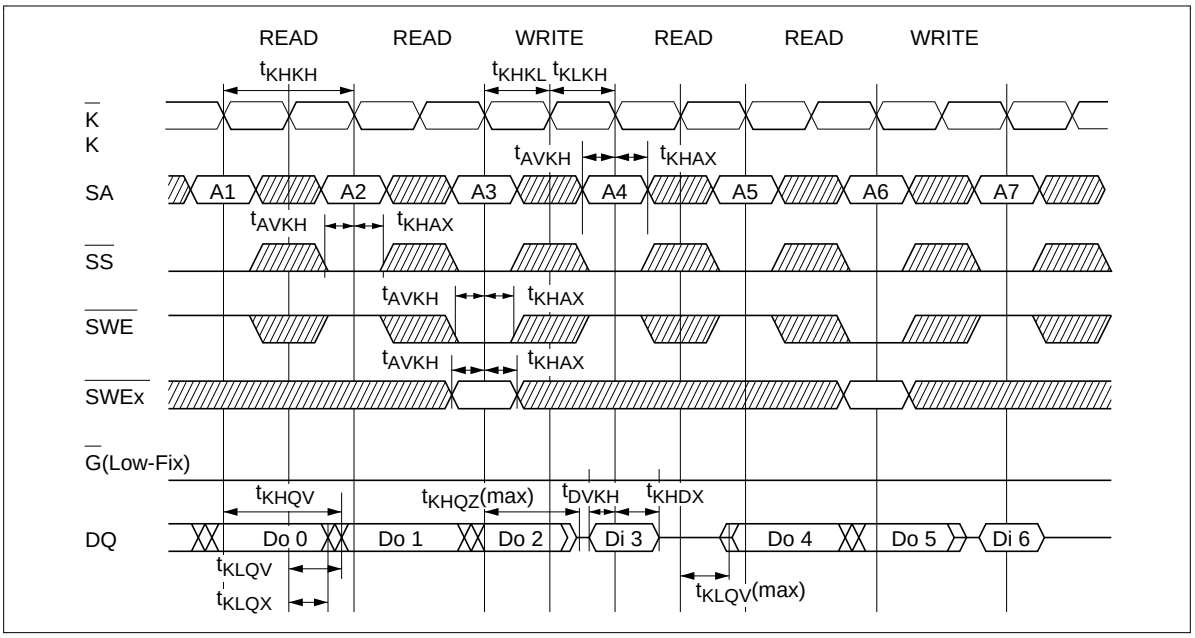
Read Cycle 3 ($\overline{G}$ Controlled)



Write Cycle


tKHKH
tKHKL
tKLKH
K
K
tAVKH
tKHAX
SA
A1
A2
A3
A4
SS
SWE
SWEx
G
tDVKH
tKHDX
DQ
Di 0
Di 1
Di 2
Di 3

Read-Write Cycle



(1) During this period DQ pins are in the output state so that the input signal of opposite phase to the outputs must not be applied.

Boundary Scan Test Access Port Operations

overview

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1. the HM67S18258 contains a TAP controller. Instruction resister, Boundary scan resister, Bypass and ID resister.

Test Access Port Pins

Symbol I/O	Name
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out

Notes: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. To disable the TAP, TCK must be connected to V_{SS}. TDO should be left unconnected.

TAP DC Operating Characteristics (Ta = 0°C to 70°C [Tj max = 110°C])

Parameter	Symbol	Min	Max	Note
Boundary scan Input High voltage	V_{IH}	2.0 V	V_{DD} + 0.3 V	
Boundary scan Input Low voltage	V_{IL}	–0.5 V	0.8 V	
Boundary scan Input Leakage Current	I_{LI}	–1µA	+1µA	1
Boundary scan Output Low voltage	V_{OL}		0.4 V	2
Boundary scan Output High voltage	V_{OH}	2.4 V		3

Notes: 1. $0 \leq Vin \leq V_{DD}$
2. I_{OL} = 2 mA
3. I_{OH} = –2 mA

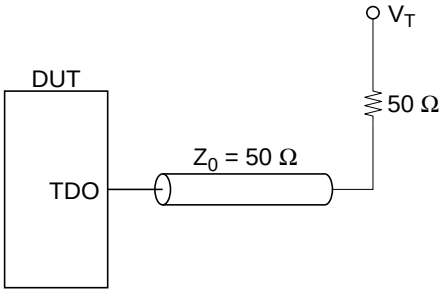
TAP AC Operating Characteristics (Ta = 0°C to 70°C [Tj max = 110 °C])

Parameter	Symbol	Min	Max	Unit
Test Clock Cycle Time	t_{THTH}	67	—	ns
Test Clock High Pulse Width	t_{THTL}	30	—	ns
Test Clock Low Pulse Width	t_{TLTH}	30	—	ns
Test Mode Select Setup	t_{MVTH}	10	—	ns
Test Mode Select Hold	t_{THMX}	10	—	ns
Capture Setup	t_{CS}	10	—	ns
Capture Hold	t_{CH}	10	—	ns
TDI Valid to TCK High	t_{DVTH}	10	—	ns
TCK High to TDI Don't Care	t_{THDX}	10	—	ns
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns
TCK Low to TDO Valid	t_{TLQV}	—	20	ns

Notes: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

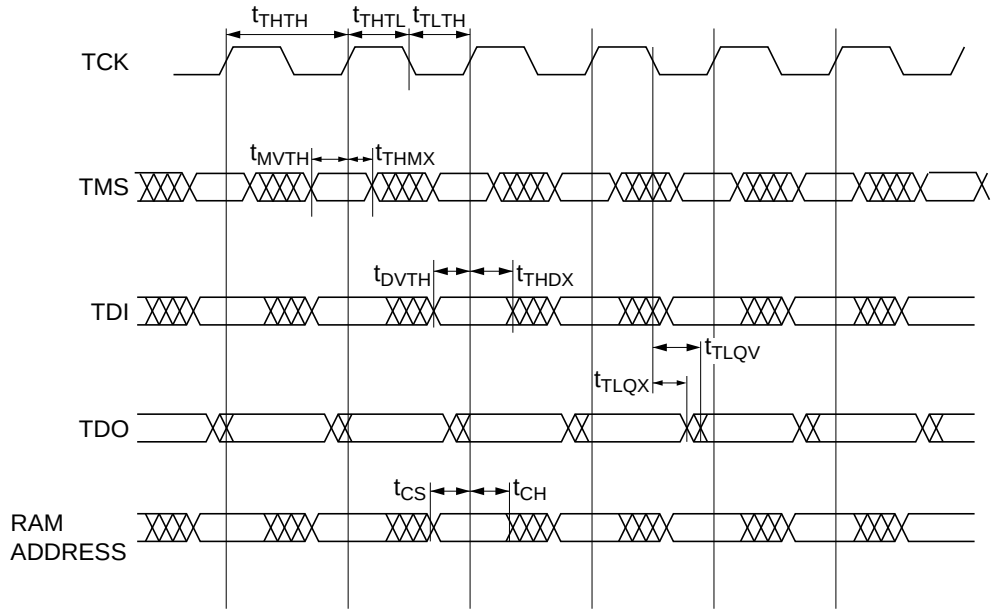
TAP AC Test Conditions

- Temperature — 0°C ≤ Ta ≤ 70°C [Tj max = 110°C]
- Input Reference Point for Single-Ended Signals — 1.5 V
- Input pulse levels — 0 to 2.5 V
- Input Rise/Fall Time — 2.0 ns typical (10% to 90%)
- Output timing reference — 1.5 V
- Test load termination supply voltage (V_T) — 1.5 V
- Output Load — See figures



boundary scan AC test Load

TAP Timing Diagram



TAP Timing Diagram

Test Access Port Registers

Register Name	Length	Symbol	Note
Instruction Register	3 bits	IR [0;2]	
Bypass Register	1 bits	BP	
ID Register	32 bits	ID [0;31]	
Boundary Scan Register	51 bits	BS [1;51]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order

Bit #	Bump ID	Signal Name	Bit #	Bump ID	Signal Name
1	5R	M2	27	2B	NC
2	6T	SA4	28	3A	SA14
3	4P	SA5	29	3C	SA15
4	6R	SA6	30	2C	SA16
5	5T	SA7	31	2A	SA17
6	7T	ZZ	32	1D	DQc0
7	7P	DQa0	33	2E	DQc1
8	6N	DQa1	34	2G	DQc2
9	6L	DQa2	35	1H	DQc3
10	7K	DQa3	36	3G	$\overline{\text{SWEc}}$
11	5L	$\overline{\text{SWEa}}$	37	4D	NC
12	4L	$\overline{\text{K}}$	38	4E	$\overline{\text{SS}}$
13	4K	K	39	4G	NC
14	4F	$\overline{\text{G}}$	40	4H	NC
15	6H	DQa4	41	4M	$\overline{\text{SWE}}$
16	7G	DQa5	42	2K	DQc4
17	6F	DQa6	43	1L	DQc5
18	7E	DQa7	44	2M	DQc6
19	6D	DQa8	45	1N	DQc7
20	6A	SA8	46	2P	DQc8
21	6C	SA9	47	3T	SA0
22	5C	SA10	48	2R	SA1
23	5A	SA11	49	4N	SA2
24	6B	NC	50	2T	SA3
25	5B	SA12	51	3R	M1
26	3B	SA13			

Notes: 1. Bit#1 is the first scan bit to exit the chip.

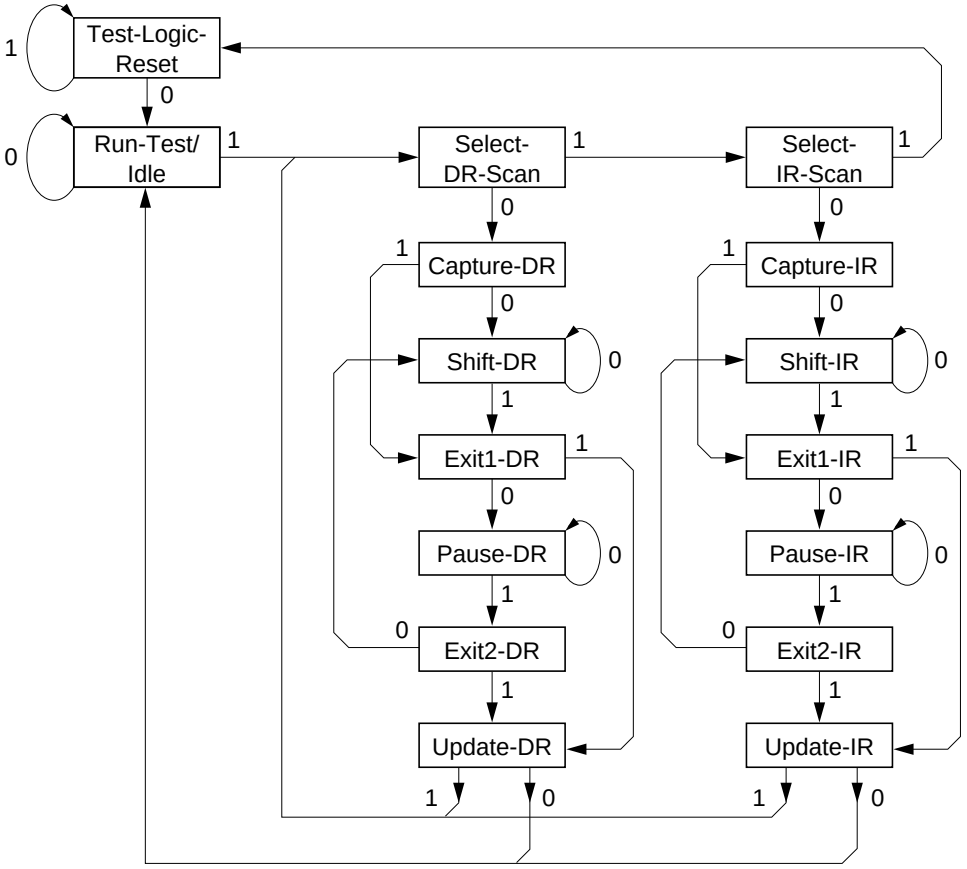
2. NC pads listed in the TABLE are represented in the Boundary Scan Register by a Place Holder. Place Holder registers are internally connected to V_{SS}.

3. The clock pins (K and $\overline{\text{K}}$) are needed as PECL differential levels. And, clock reciever generated single clock signal. This signal and its inverted signal are used for Boundary Scan Register input signal.

ID register

Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	0	1	1	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	Vendor Revision No.				4M, 16M Depth		Depth			4M, 16M Width		Width			Use in the future						Vendor ID No.											Fix

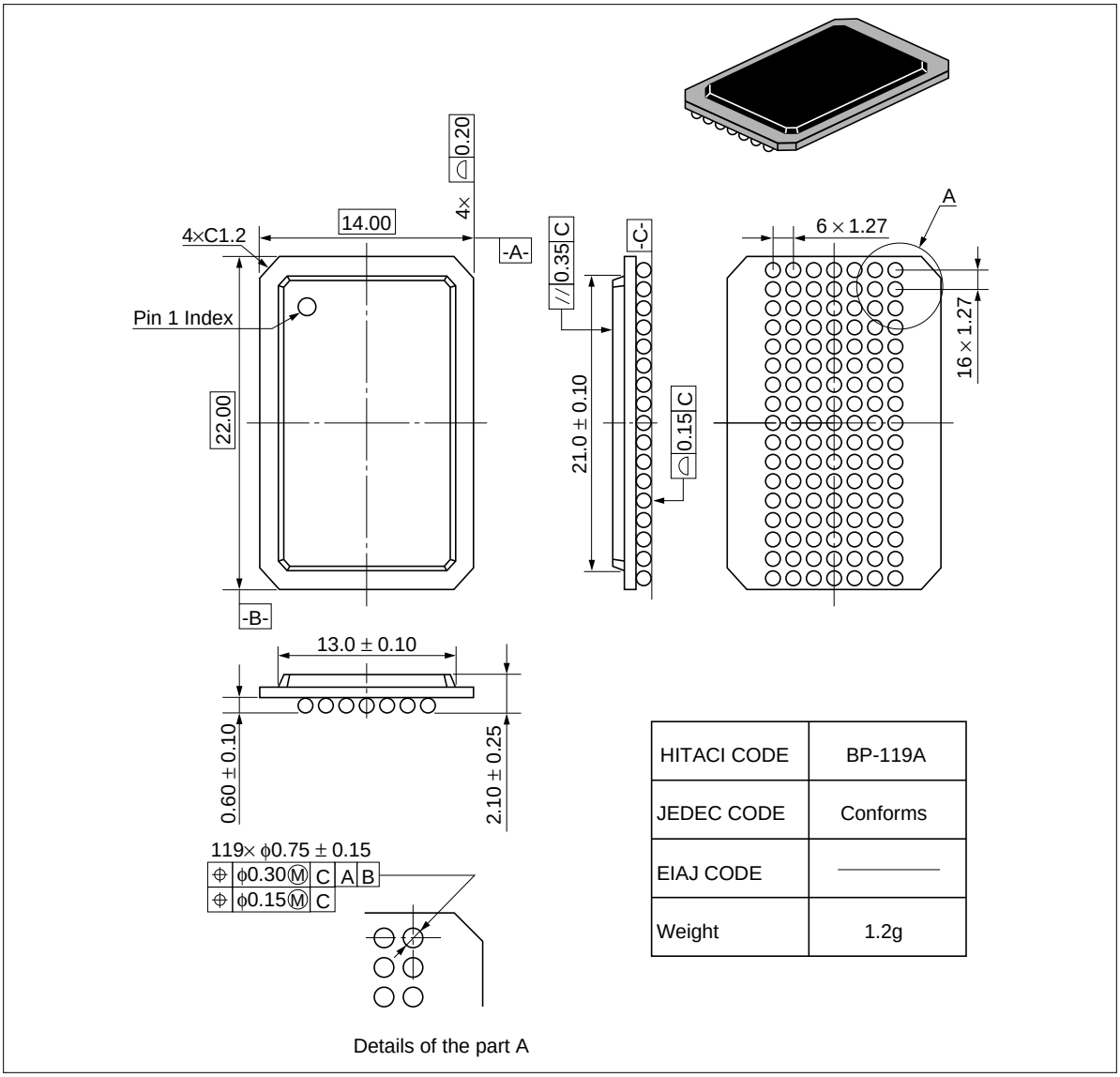
TAP Controller State Diagram



Note: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Outline

HM67S18258BP (BP-119A) **Unit : mm**



HITACI CODE	BP-119A
JEDEC CODE	Conforms
EIAJ CODE	————
Weight	1.2g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 1, 1996	Initial issue	—	K.Mitsumoto
1	Feb. 21, 1997	P1. 3.3V± 0.1V Operation to 3.3V± 5% Operation Change HM67S18258BP-7H to HM67S18258BP-7 V_{DD}min 3.2 to 3.135 V_{DD}max 3.4 to 3.465 V_{DDQ}min 3.2/.6 to 3.135/2.375 V_{DDQ}max 3.4/2.6 to 3.465/2.75 I_{DD}max 500 to 600 I_{OH} 2mA to - 2mA I_{OL} - 2mA to 2mA P.7 Change termination load t_{KHKL} 3.2 to 2.0 t_{KLKH} 3.2 to 2.0 Add t_{KHQZ}min Add Note 2 Delete Soft Error Rate	(Y. Matsui)	S.Nakazato
2	Nov. 18, 1997	BP-119 to BP-119A	(Y. Matsui)	S. Nakazato