BURR-BROWN®

ADS824

SpeedPLUS™ 10-Bit, 70MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SNR: 59dB
- HIGH SFDR: 70dB
- LOW POWER: 315mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE: 1Vp-p or 2Vp-p
- LOW DNL: 0.3LSB
- SINGLE +5V SUPPLY OPERATION
- +3V DIGITAL OUTPUT CAPABILITY
- POWER DOWN: 20mW
- 28-LEAD SSOP PACKAGE

APPLICATIONS

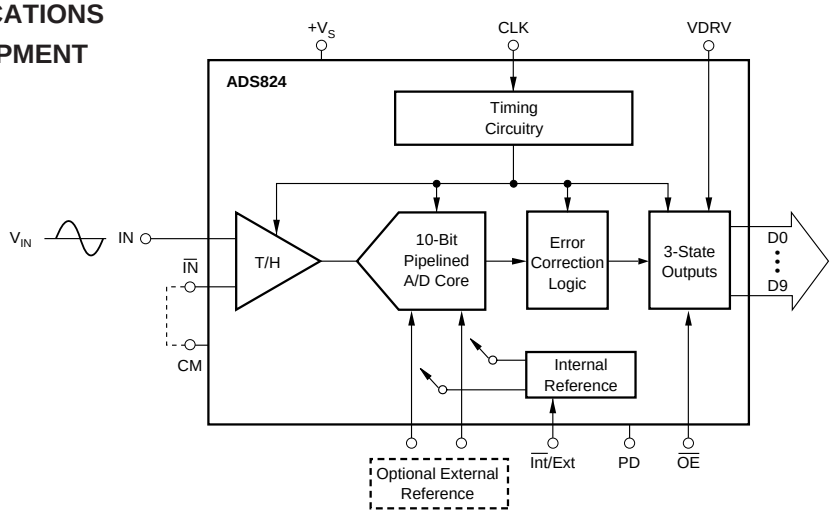
- MEDICAL IMAGING
- HDTV VIDEO DIGITIZING
- COMMUNICATIONS
- TEST EQUIPMENT

DESCRIPTION

The ADS824 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes a 10-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where full scale range adjustment is required.

The ADS824 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS824 offers power dissipation of 315mW and also provides a power-down mode, thus reducing power dissipation to only 20mW.

The ADS824 is specified at a maximum sampling frequency of 70MHz and a single-ended input range of 1.5V to 3.5V. The ADS824 is available in a 28-lead SSOP package and is pin compatible with the 10-bit, 40MHz ADS822 and the 10-bit, 60MHz ADS823.



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SPECIFICATIONS

At T_A = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 70MHz, external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS824E MIN	ADS824E TYP	ADS824E MAX	UNITS
RESOLUTION			10 Guaranteed		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Standard Single-Ended Input Range	2Vp-p	1.5		3.5	V
Optional Single-Ended Input Range	1Vp-p	2		3	V
Common-Mode Voltage			2.5		V
Optional Differential Input Range	2Vp-p	2		3	V
Analog Input Bias Current			1		µA
Input Impedance			1.25 || 5		MΩ || pF
Track-Mode Input Bandwidth	–3dBFS		300		MHz
CONVERSION CHARACTERISTICS					
Sample Rate		10k		70M	Samples/s
Data Latency			5		Clk Cyc
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 1MHz			±0.3	±1.0	LSB
f = 10MHz			±0.3		LSB
No Missing Codes			Guaranteed		
Integral Nonlinearity Error, f = 1MHz			±0.5	±3.0	LSBs
Spurious Free Dynamic Range[1]	Referred to Full Scale				
f = 1MHz			70		dBFS[2]
f = 10MHz		60	68		dBFS
Two-Tone Intermodulation Distortion[3]					
f = 4.5MHz and 5.5MHz (–7dB each tone)			–63.4		dBc
Signal-to-Noise Ratio (SNR)	Referred to Full Scale				
f = 1MHz			59		dB
f = 10MHz		55	59		dB
Signal-to-(Noise + Distortion) (SINAD)	Referred to Full Scale				
f = 1MHz			58		dB
f = 10MHz		50	58		dB
Effective Number of Bits[4], f = 1MHz			9.3		Bits
Output Noise	Input Grounded		0.2		LSBs rms
Aperture Delay Time			3		ns
Aperture Jitter			1.2		ps rms
Overvoltage Recovery Time			2		ns
Full-Scale Step Acquisition Time			5		ns
DIGITAL INPUTS					
Logic Family			CMOS-Compatible		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current[5] (V_{IN} = 5V)				100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+3.5			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS-Compatible		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA)	VDRV = 5V			+0.1	V
Low Output Voltage, (I_{OL} = 1.6mA)				+0.2	V
High Output Voltage, (I_{OH} = 50µA)		+4.9			V
High Output Voltage, (I_{OH} = 0.5mA)		+4.8			V
Low Output Voltage, (I_{OL} = 50µA)	VDRV = 3V			+0.1	V
High Output Voltage, (I_{OH} = 50µA)		+2.8			V
3-State Enable Time	$\overline{OE}$ = L		20	40	ns
3-State Disable Time	$\overline{OE}$ = H		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)					
Zero Error (Referred to –FS)	at 25°C		±0.5	±3.0	%FS
Zero Error Drift (Referred to –FS)			12		ppm/°C
Gain Error[6]	at 25°C		±1.5	±2.5	%FS
Gain Error Drift[6]			38		ppm/°C
Gain Error[7]	at 25°C		±0.75	±1.5	%FS
Gain Error Drift[7]			20		ppm/°C
Power Supply Rejection of Gain	ΔV_S = ±5%		68		dB
REFT Tolerance	Deviation from Ideal 3.5V		±10	±25	mV
REFB Tolerance	Deviation From Ideal 1.5V		±10	±25	mV
External REFT Voltage Range		REFB + 0.8	3.5	V_S – 1.25	V
External REFB Voltage Range		1.25	1.5	REFT – 0.8	V
Reference Input Resistance			1.6		kΩ

SPECIFICATIONS (CONT)

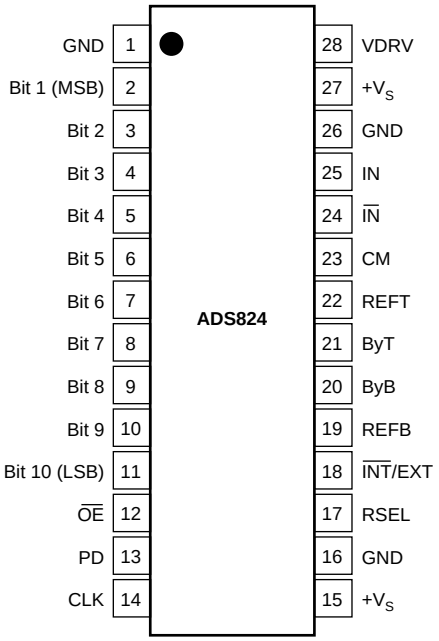
At T_A = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 70MHz, external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS824E			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		66		mA
Output Driver Supply Current (VDRV)			9		mA
Power Dissipation: VDRV = 5V	External Reference		330	375	mW
VDRV = 3V	External Reference		315		mW
VDRV = 5V	Internal Reference		345		mW
VDRV = 3V	Internal Reference		335		mW
Power Down	Operating		20		mW
Thermal Resistance, θ_{JA}					
28-Lead SSOP			89		°C/W

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally. (6) Includes internal reference. (7) Excludes internal reference.

PIN CONFIGURATION

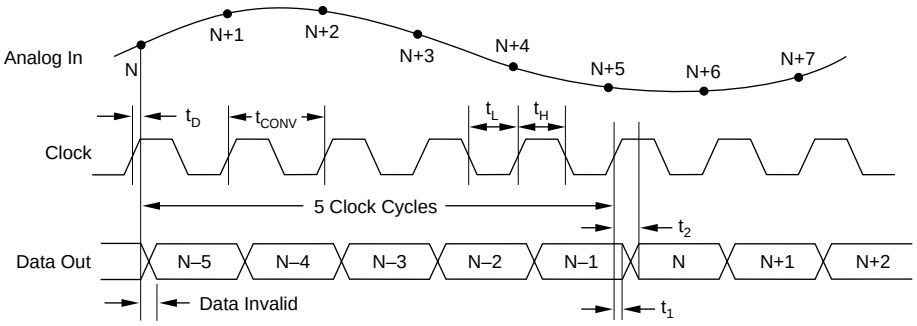
Top View **SSOP**



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	Bit 1	Data Bit 1 (D9) (MSB)
3	Bit 2	Data Bit 2 (D8)
4	Bit 3	Data Bit 3 (D7)
5	Bit 4	Data Bit 4 (D6)
6	Bit 5	Data Bit 5 (D5)
7	Bit 6	Data Bit 6 (D4)
8	Bit 7	Data Bit 7 (D3)
9	Bit 8	Data Bit 8 (D2)
10	Bit 9	Data Bit 9 (D1)
11	Bit 10	Data Bit 10 (D0) (LSB)
12	$\overline{OE}$	Output Enable. HI = high impedance state. LO = normal operation (internal pull-down resistor)
13	PD	Power Down. HI = power down; LO = normal
14	CLK	Convert Clock Input
15	$+V_S$	+5V Supply
16	GND	Ground
17	RSEL	Input Range Select. HI = 2Vp-p; LO = 1Vp-p
18	$\overline{INT}$/EXT	Reference Select. HI = external; LO = internal
19	REFB	Bottom Reference
20	ByB	Bottom Ladder Bypass
21	ByT	Top Ladder Bypass
22	REFT	Top Reference
23	CM	Common-Mode Voltage Output
24	$\overline{IN}$	Complementary Input (–)
25	IN	Analog Input (+)
26	GND	Ground
27	$+V_S$	+5V Supply
28	VDRV	Output Logic Driver Supply Voltage

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	13.4		100µs	ns
t_L	Clock Pulse Low	6.4	6.7		ns
t_H	Clock Pulse High	6.4	6.7		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA
ADS824E	SSOP-28	324	–40°C to +85°C	ADS824E	ADS824E	Rails
"	"	"	"	"	ADS824E/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of ADS824E/iK" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

DEMO BOARD ORDERING INFORMATION

PRODUCT	DEMO BOARD
ADS824E	DEM-ADS824E

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	–0.3V to ($+V_S$ + 0.3V)
Logic Input	–0.3V to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

ELECTROSTATIC DISCHARGE SENSITIVITY

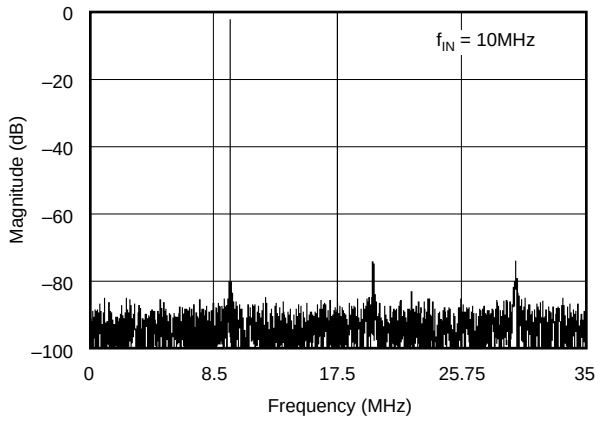
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

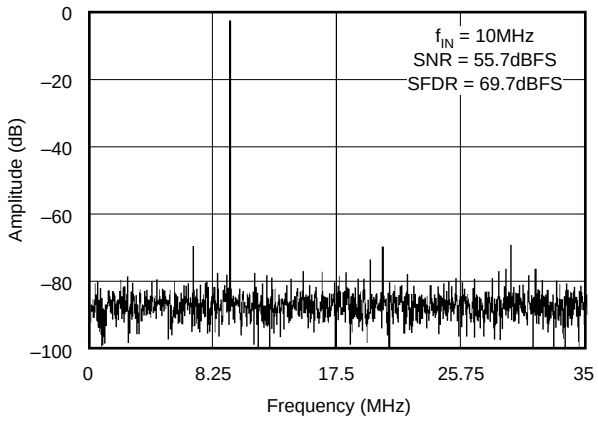
TYPICAL PERFORMANCE CURVES

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, and sampling rate = 70MHz, external reference, unless otherwise noted.

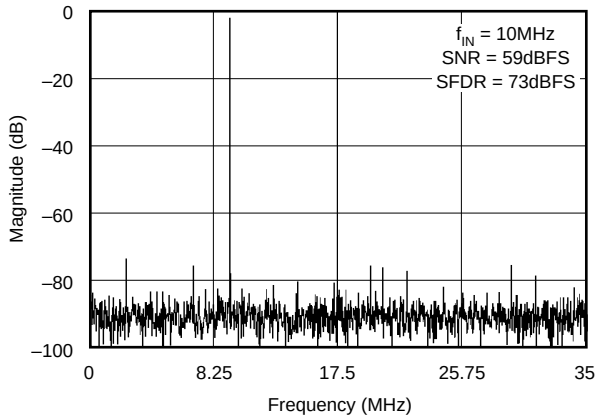
SPECTRAL PERFORMANCE



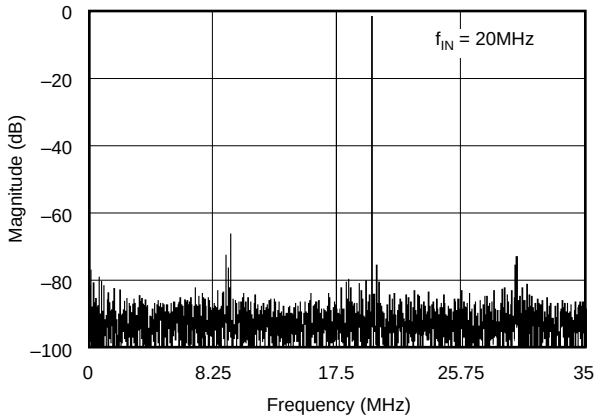
SPECTRAL PERFORMANCE
(Single-Ended Input, 1Vp-p)



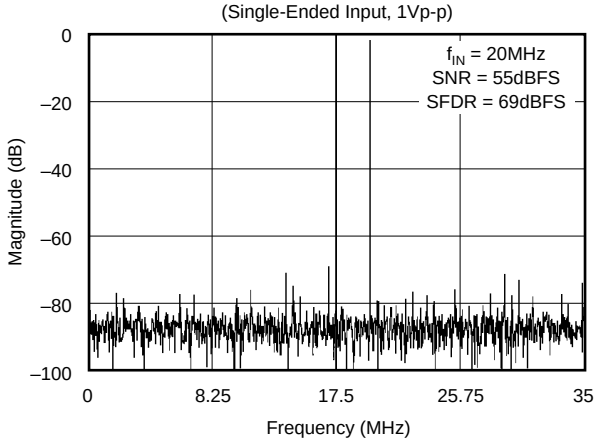
SPECTRAL PERFORMANCE
(Differential Input, 2Vp-p)



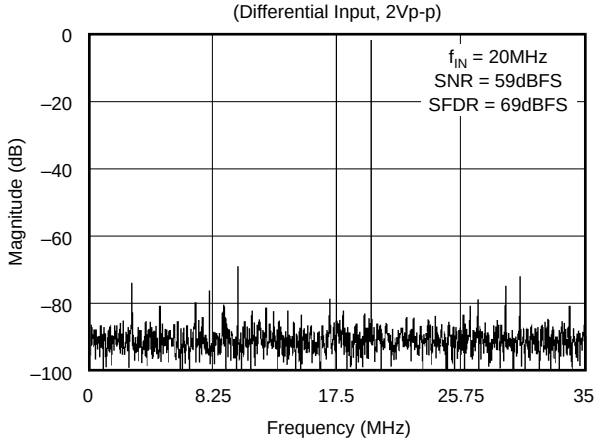
SPECTRAL PERFORMANCE



SPECTRAL PERFORMANCE
(Single-Ended Input, 1Vp-p)



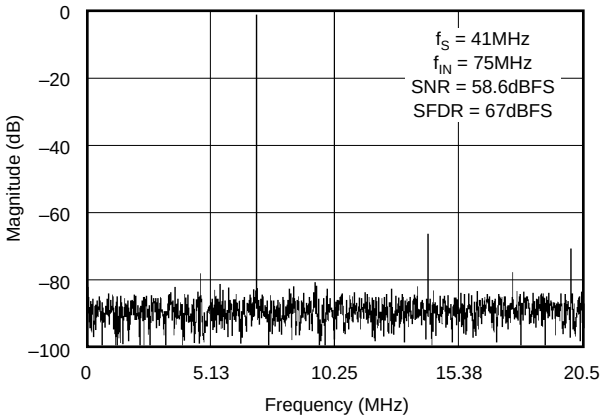
SPECTRAL PERFORMANCE
(Differential Input, 2Vp-p)



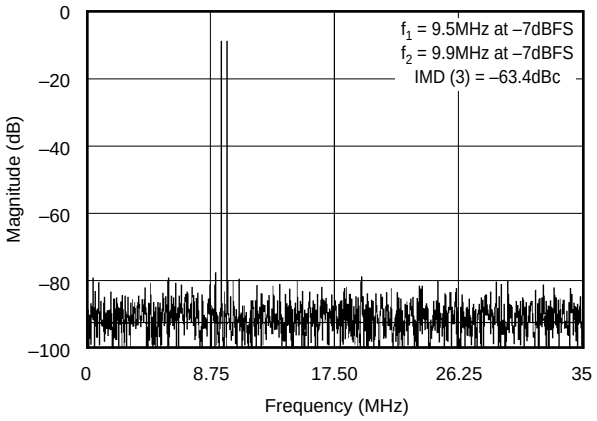
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, and sampling rate = 70MHz, external reference, unless otherwise noted.

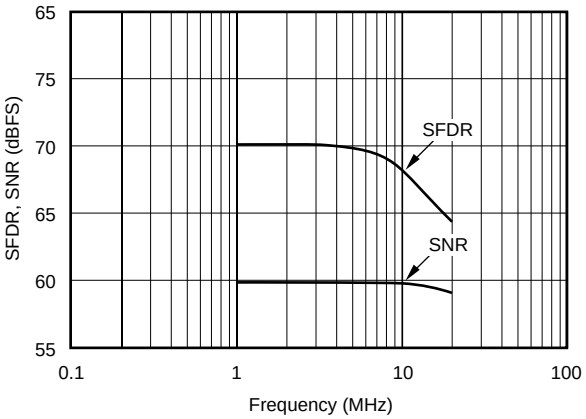
UNDERSAMPLING
(Differential Input, 2Vp-p)



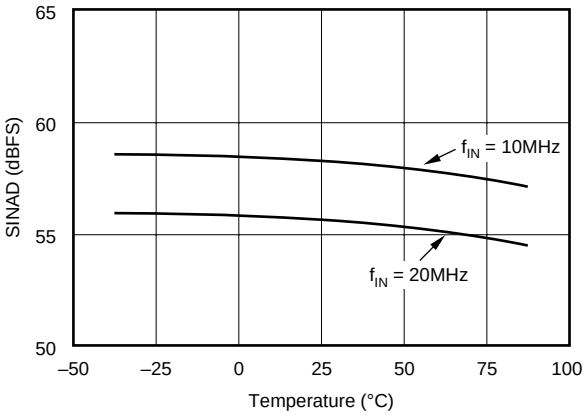
TWO-TONE INTERMODULATION DISTORTION
(Differential Input, 2Vp-p)



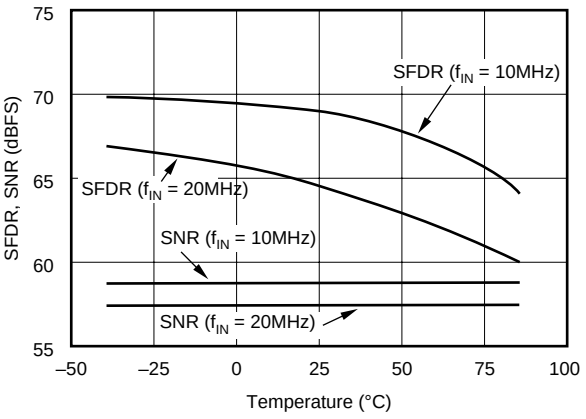
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



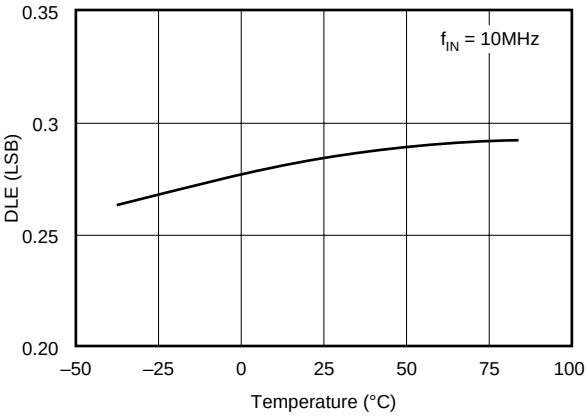
SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



DYNAMIC PERFORMANCE vs TEMPERATURE



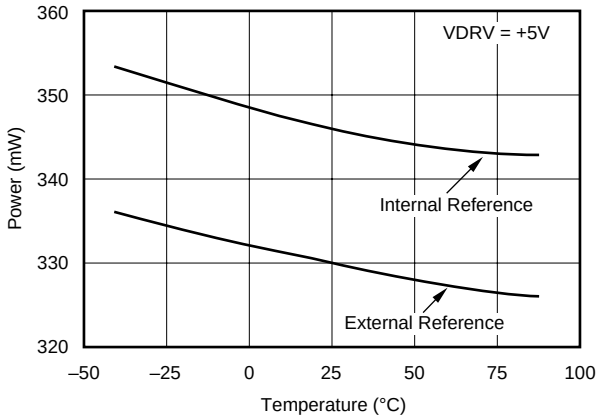
DIFFERENTIAL LINEARITY ERROR
vs TEMPERATURE



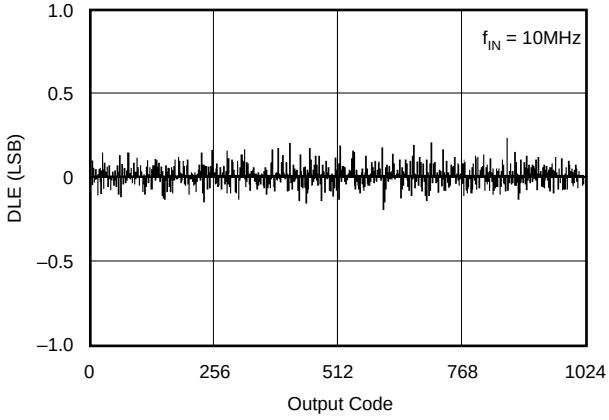
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, and sampling rate = 70MHz, external reference, unless otherwise noted.

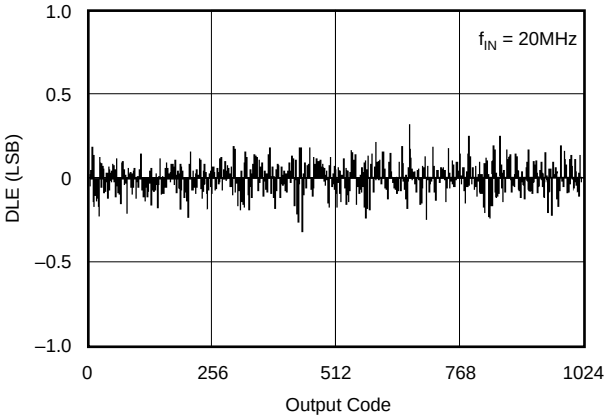
POWER DISSIPATION vs TEMPERATURE



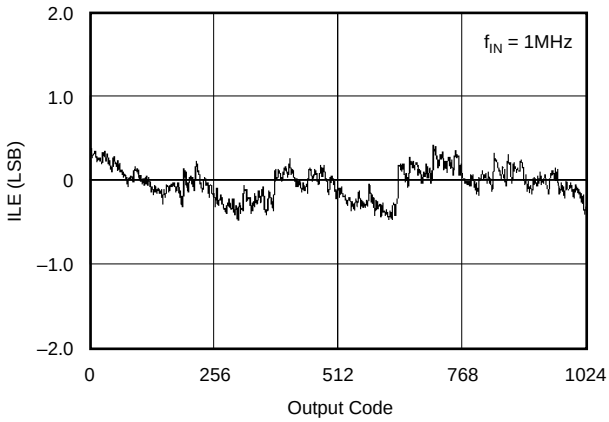
DIFFERENTIAL LINEARITY ERROR



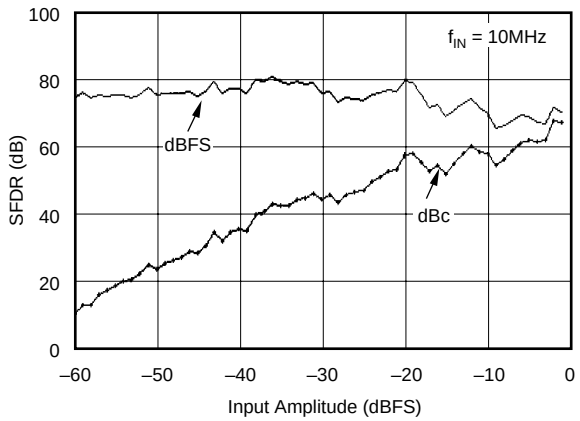
DIFFERENTIAL LINEARITY ERROR



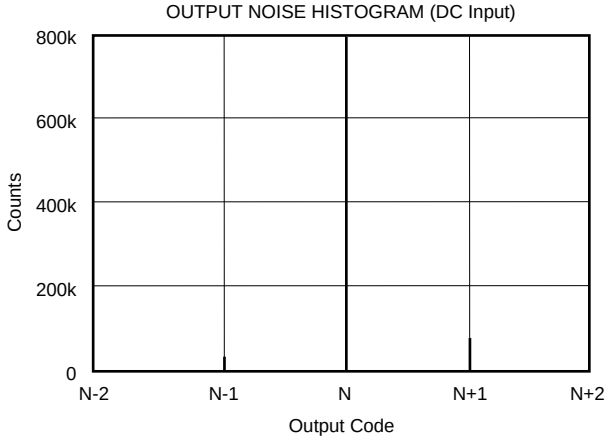
INTEGRAL LINEARITY ERROR



SWEPT POWER SFDR



OUTPUT NOISE HISTOGRAM (DC Input)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS824 is a high-speed, CMOS analog-to-digital converter which employs a pipelined converter architecture consisting of 9 internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 10-bit level. The output data becomes valid on the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 5 clock cycles.

The analog input of the ADS824 is a differential track and hold (see Figure 1). The differential topology along with tightly matched capacitors produce a high level of ac-performance while sampling at very high rates.

The ADS824 allows its analog inputs to be driven either single-ended or differentially. The typical configuration for the ADS824 is for the single-ended mode in which the input track-and-hold performs a single-ended-to-differential conversion of the analog input signal.

Both inputs (IN, $\overline{IN}$) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

The following application discussion focuses on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS824 are characterized using the single-ended mode of operation.

DRIVING THE ANALOG INPUT

The ADS824 achieves excellent ac performance either in the single-ended or differential mode of operation. The selection for the optimum interface configuration will depend on the individual application requirements and system structure. For example, communications applications often process a band of frequencies that do not include DC, whereas in imaging applications, the previously restored DC level must be maintained correctly up to the A/D converter. Features on the ADS824 such as the input range select (RSEL pin) or the option for an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the ADS824 should be configured such that the application objectives are met while observing the headroom requirements of the driving amplifier in order to yield the best overall performance.

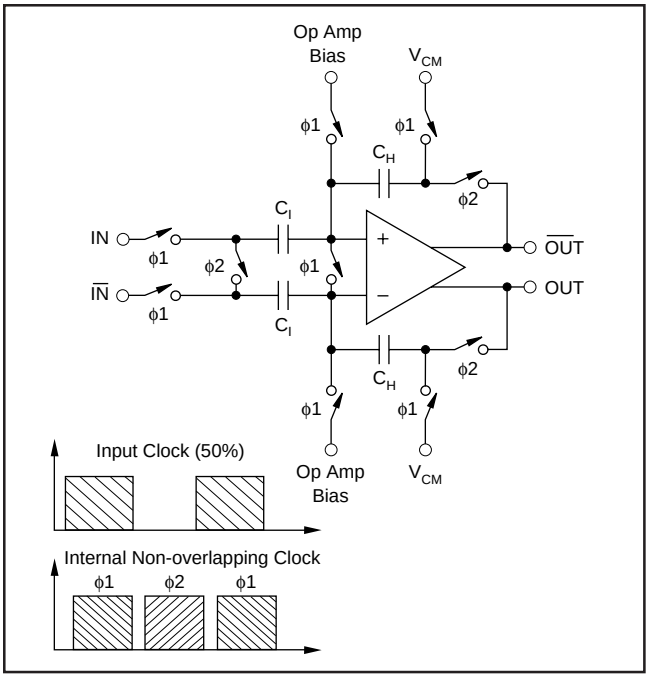


FIGURE 1. Simplified Circuit of Input Track-and-Hold with Timing Diagram.

INPUT CONFIGURATIONS

AC-Coupled, Single-Supply Interface

Figure 2 shows the typical circuit for an ac-coupled analog input configuration of the ADS824 while all components are powered from a single +5V supply.

With the RSEL pin connected high, the full-scale input range is set to 2Vp-p. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3.5V and +1.5V, respectively. Two resistors (2x 1.0kΩ) are used to create a common-mode voltage (V_{CM}) of approximately +2.5V to bias the inputs of the driving amplifier A1. Using the OPA680 on a single +5V supply, its ideal common-mode point is at +2.5V, which coincides with the recommended common-mode input level for the ADS824. This obviates the need of a coupling capacitor between the amplifier and the converter. Even though the OPA680 has an ac gain of +2, the dc gain is only +1 due to the blocking capacitor at resistor R_G.

The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS824 will be beneficial in almost all interface configurations. This will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor, in combination with the 10pF capacitor, establishes a passive low-pass filter, limiting the bandwidth for the wideband noise thus, help improving the SNR performance.

AC-Coupled, Dual Supply Interface

The circuit provided in Figure 3 shows typical connections for the analog input in case the selected amplifier operates on dual supplies. This might be necessary to take full advantage of very low distortion operational amplifiers, like the OPA642. The advantage is that the driving amplifier can be operated with a ground referenced bipolar signal swing. This will keep the distortion performance at its lowest since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. By capacitively coupling the single-ended signal to the input of the ADS824, its common-mode requirements can easily be satisfied with two resistors connected between the top and bottom reference.

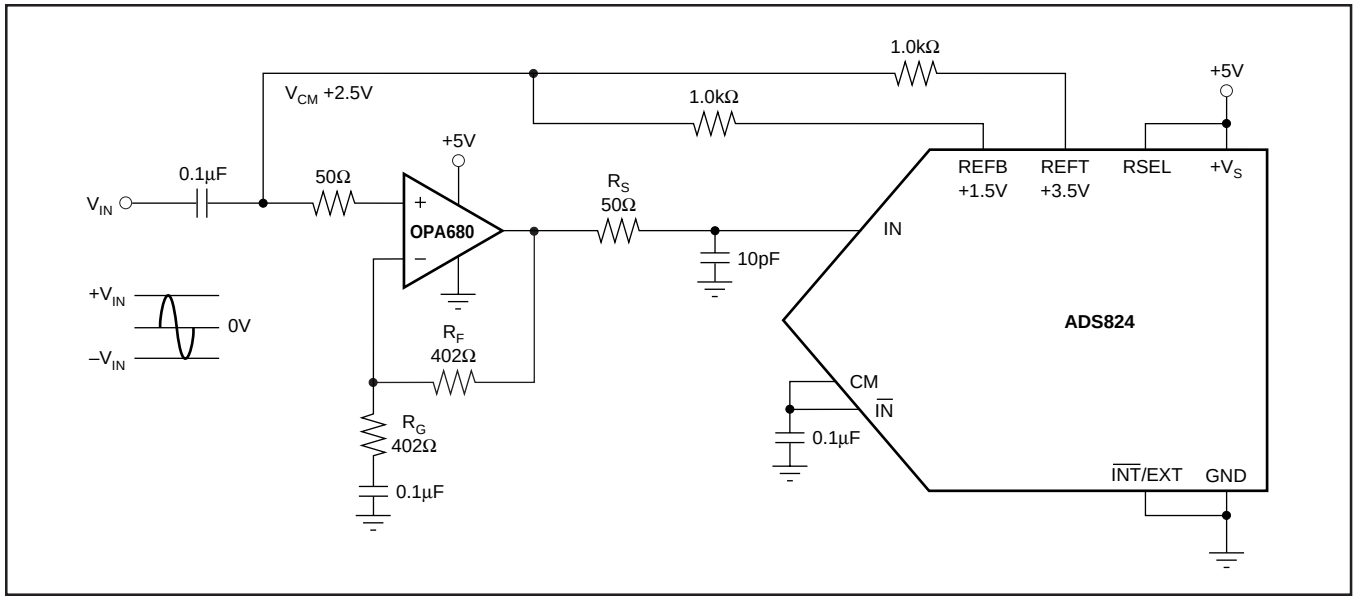


FIGURE 2. AC-Coupled Input Configuration for a 2Vp-p Full-Scale Range and a Common-Mode Voltage, V_{CM}, at +2.5V Derived From The Internal Top (REFT) and Bottom Reference (REFB).

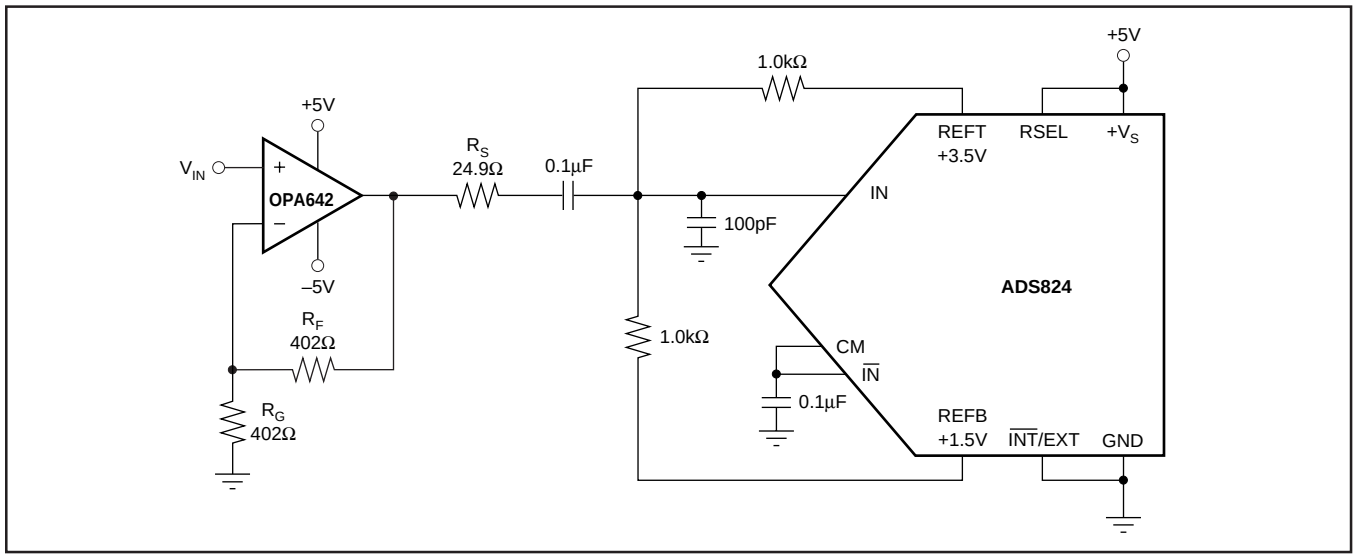


FIGURE 3. AC-Coupling the Dual Supply Amplifier OPA642 to the ADS823 for a 2Vp-p Full-Scale Input Range.

For applications requiring the driving amplifier to provide a signal amplification, with a gain ≥ 5, consider using decompensated voltage-feedback op amps, like the OPA643, or current-feedback op amps like the OPA681 and OPA658.

DC-coupled with Level Shift

Several applications may require that the bandwidth of the signal path include DC, in which case, the signal has to be DC-coupled to the A/D converter. In order to accomplish this, the interface circuit has to provide a DC level shift to the analog input signal. The circuit shown in Figure 4 employs a dual op amp, A1, to drive the input of the ADS824 and level shift the signal to be compatible with the selected input range. With the RSEL pin tied to the supply and the $\overline{INT}$/EXT pin to ground, the ADS824 is configured for a 2Vp-p input range and uses the internal references. The complementary input ($\overline{IN}$) may be appropriately biased using the +2.5V common-mode voltage available at the CM pin. One-half of amplifier A1 buffers the REFB pin and drives the voltage divider R_1, R_2. Because of the op amp's noise gain of +2V/V, assuming $R_F = R_{IN}$, the common-mode voltage (V_{CM}) has to be re-scaled to +1.25. This results in the correct DC level of +2.5V for the signal input (IN). Any DC voltage differences between the IN and $\overline{IN}$ inputs of the ADS824 effectively produces an offset, which can be corrected for by adjusting the resistor values of the divider, R_1 and R_2. The selection criteria for a suitable op amp should include the supply voltage, input bias current, output voltage swing, distortion, and noise specification. Note that in this example, the overall signal phase is inverted. To re-establish the original signal polarity, it is always possible to interchange the IN and $\overline{IN}$ connections.

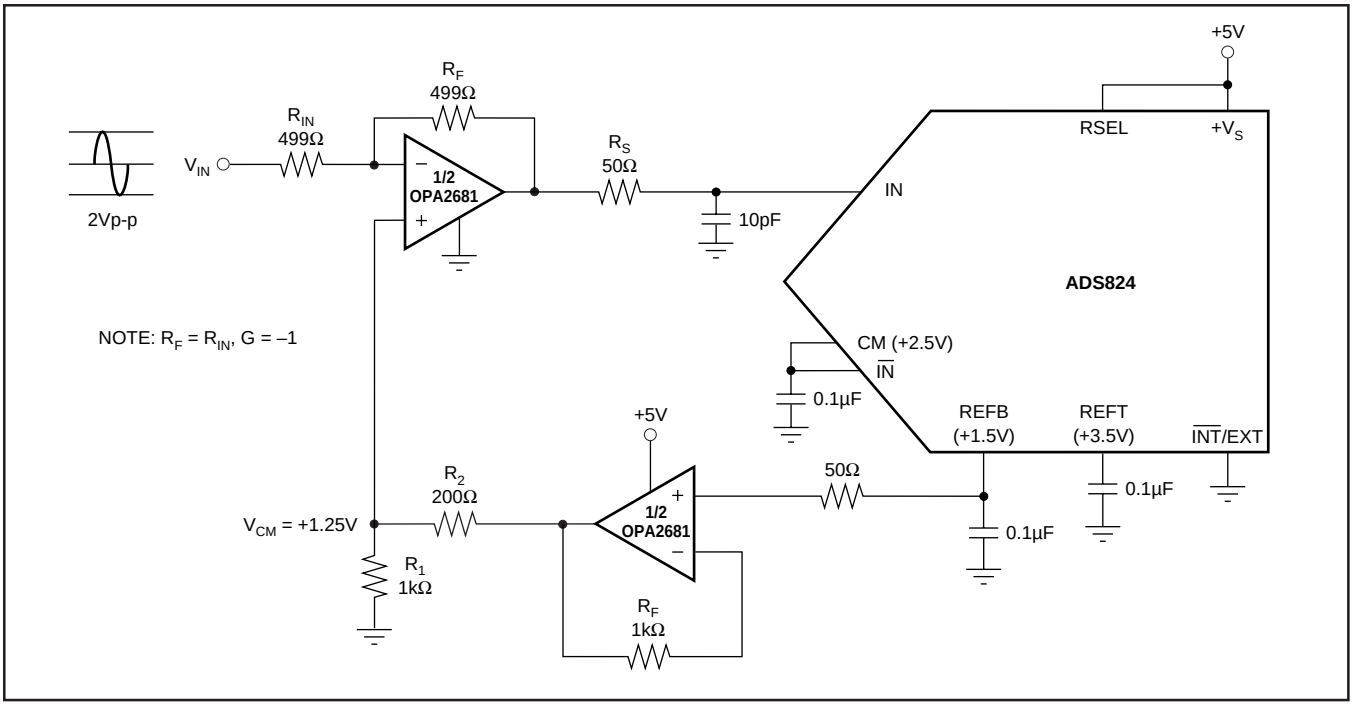


FIGURE 4. DC-Coupled Interface Circuit with Level Shifting Using Dual Current-Feedback Amplifier OPA2681.

SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (Transformer Coupled)

If the application requires a signal conversion from a single-ended source to feed the ADS824 differentially, a RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode, both inputs of the ADS824 see matched impedances, and the differential signal swing can be reduced to half of the swing required for single-ended drive. Figure 5 shows the schematic for the suggested transformer-coupled interface circuit. The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_T) should be calculated using the equation $R_T = n^2 \times R_G$ to match the source impedance (R_G) for good power transfer and Voltage Standing Wave Ratio (VSWR).

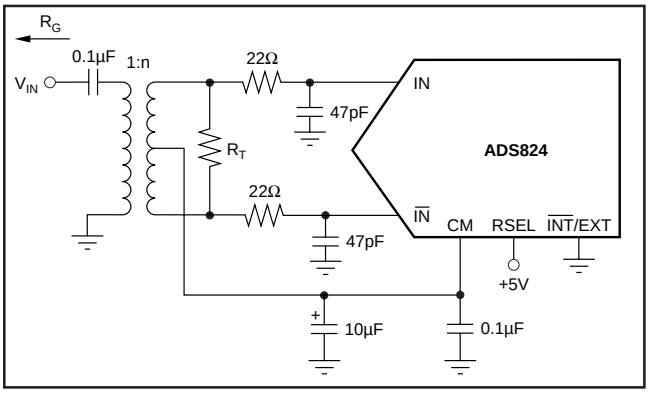


FIGURE 5. Transformer Coupled Input.

REFERENCE OPERATION

Figure 6 depicts the simplified model of the internal reference circuit. The internal blocks are the bandgap voltage reference, the drivers for the top and bottom reference, and

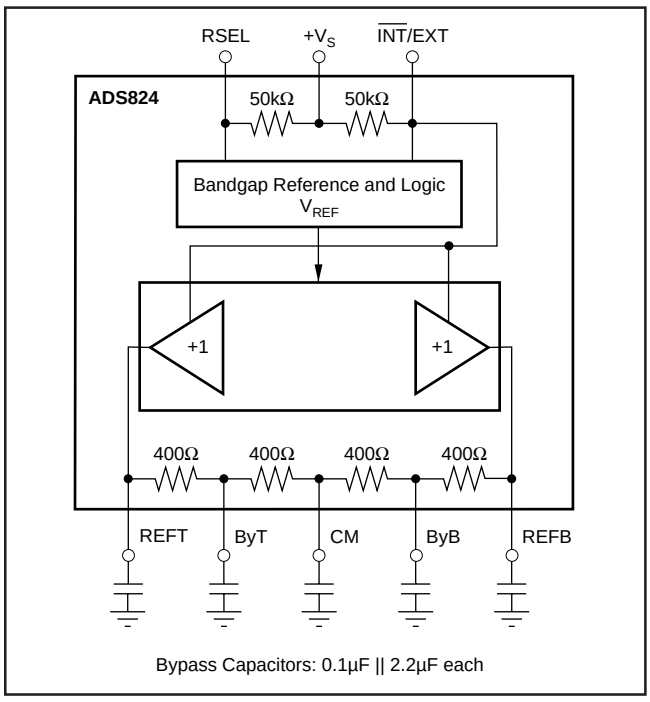


FIGURE 6. Equivalent Reference Circuit with Recommended Reference Bypassing.

the resistive reference ladder. The bandgap reference circuit includes logic functions that allows setting the analog input swing of the ADS824 to either a 1Vp-p or 2Vp-p full-scale range by simply tying the RSEL pin to a Low or High potential, respectively. While operating the ADS824 in the external reference mode, the buffer amplifiers for the REFT and REFB are disconnected from the reference ladder.

As shown, the ADS824 has internal 50kΩ pull-up resistors at the range select pin (RSEL) and reference select pin ($\overline{INT}$/EXT). Leaving these pins open configures the ADS824 for a 2Vp-p input range and external reference operation. Setting the ADS824 up for internal reference mode requires to bringing the $\overline{INT}$/EXT pin low.

The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. The resistor ladder of the ADS824 is divided into several segments and has two additional nodes, ByT and ByB, which are brought out for external bypassing only (Figure 6). To ensure proper operation with any reference configurations, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum. All bypassing capacitors should be located as close to their respective pins as possible.

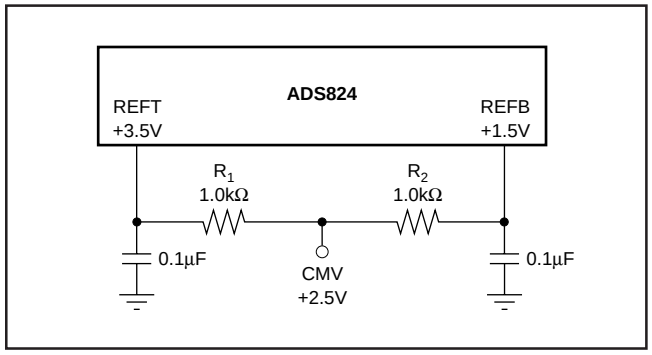


FIGURE 7. Alternative Circuit to Generate CM Voltage.

The common-mode voltage available at the CM-pin may be used as a bias voltage to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternative way of generating a common-mode voltage is given in Figure 7. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode voltage, CMV, will appear at the midpoint.

EXTERNAL REFERENCE OPERATION

For even more design flexibility, the internal reference can be disabled and an external reference voltage be used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. Especially in multichannel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

The external references can vary as long as the value of the external top reference $REFT_{EXT}$ stays within the range of (V_S – 1.25V) and (REFB + 0.8V), and the external bottom reference $REFB_{EXT}$ stays within 1.25V and (REFT – 0.8V). See Figure 8.

DIGITAL INPUTS AND OUTPUTS

Clock Input Requirements

Clock jitter is critical to the SNR performance of high speed, high resolution A/D converters. Clock jitter leads to aperture jitter (t_A), which adds noise to the signal being converted. The ADS824 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is

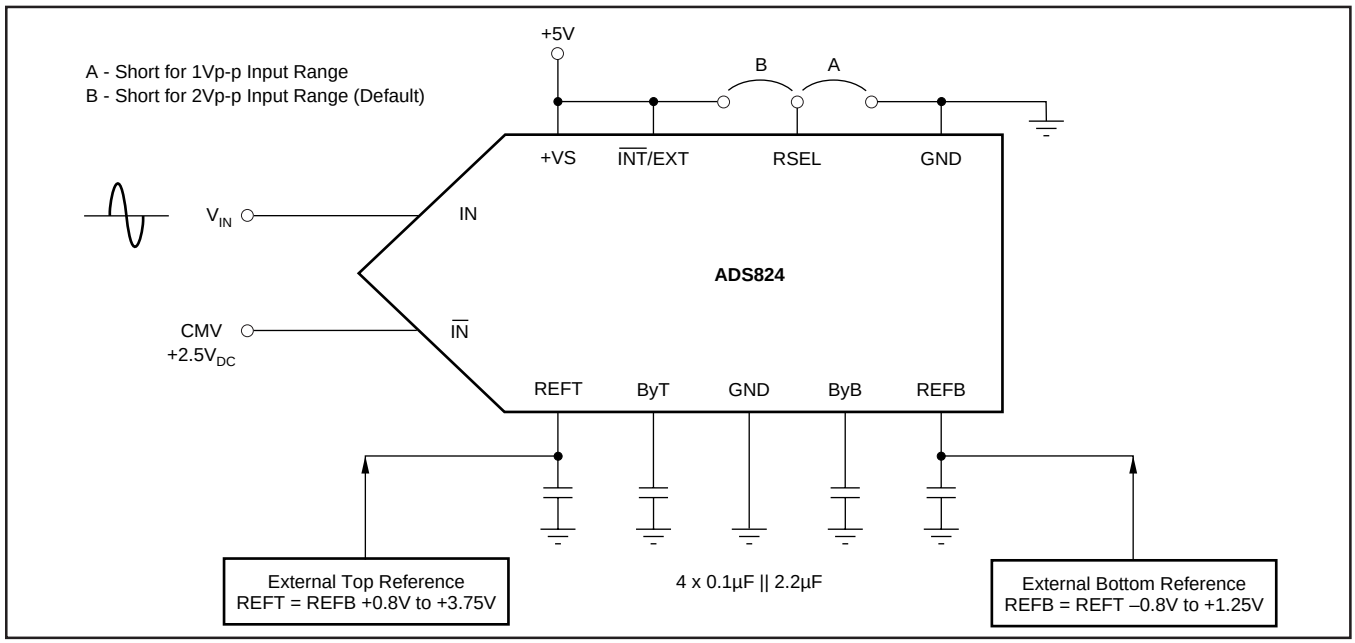


FIGURE 8. Configuration Example for External Reference Operation.

given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$Jitter\ SNR = 20\log\frac{1}{2\pi f_{IN}\ t_A}\ rms\ signal\ to\ rms\ noise$$

where: f_{IN} is input signal frequency
t_A is rms clock jitter

Special consideration should be given to clock jitter, particularly in undersampling applications. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of performance. When digitizing at high sampling rates, the clock should have 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less.

Digital Outputs

The output data format of the ADS824 is in positive Straight Offset Binary code, see Tables I and II. This format can easily be converted into the Binary Two's Complement code by inverting the MSB.

It is recommended to keep the capacitive loading on the data lines as low as possible (≤ 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS824 and affect the performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS824 from any digital noise activities on the bus coupling back high frequency noise.

SINGLE-ENDED INPUT ($\overline{IN}$ = CMV)	STRAIGHT OFFSET BINARY (SOB)
+FS –1LSB (IN = REFT)	11 1111 1111
+1/2 Full Scale	11 0000 0000
Bipolar Zero (IN = CMV)	10 0000 0000
–1/2 Full Scale	01 0000 0000
–FS (IN = REFB)	00 0000 0000

TABLE I. Coding Table for Single-Ended Input Configuration with $\overline{IN}$ Tied to the Common-Mode Voltage (CMV).

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)
+FS –1LSB (IN = +3V, $\overline{IN}$ = +2V)	11 1111 1111
+1/2 Full Scale	11 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = CMV)	10 0000 0000
–1/2 Full Scale	01 0000 0000
–FS (IN = +2V, $\overline{IN}$ = +3V)	00 0000 0000

TABLE II. Coding Table for Differential Input Configuration and 2Vp-p Full-Scale Range.

Digital Output Driver (VDRV)

The ADS824 features a dedicated supply pin for the output logic drivers, VDRV, which is not internally connected to the other supply pins. By setting the voltage at VDRV to +5V or +3V, the ADS824 produces corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS824 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line, which may affect the ac performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi-filter.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS824 should be treated as an analog component. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS824 are internally joined together, obviating the design of split ground planes. The ground pins (1, 16, 26) should directly connect to an analog ground plane, which covers the PC board area around the converter. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Because of its high sampling rate the, ADS824 generates high frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins be sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the ADS824. In most cases, 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor (1µF to 22µF) should be placed on the PC board in proximity of the converter circuit.

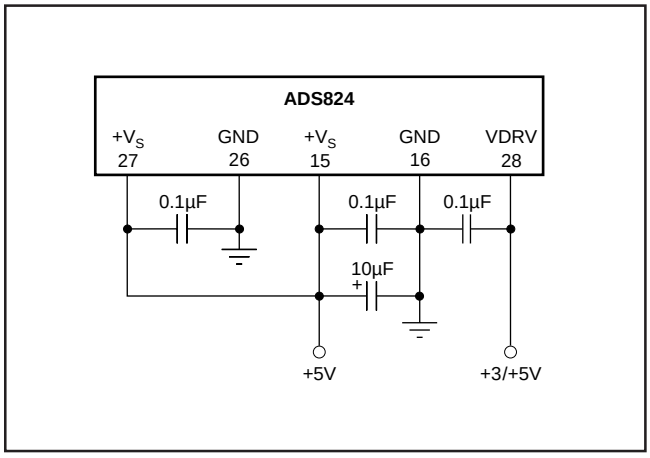


FIGURE 9. Recommended Bypassing for the Supply Pins.