A novel, cost-effective technique for converting VRM8.X VID to VRM9.0 compatible VID

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Abstract

Since AIC1569A has been designed to meet the Pentium II Processor, the equipped voltage level range is from 3.5V to 1.3V. As the trend of new generation CPU core voltage decreasing goes on, the only and also major problem of VID setting is the mismatch with (the VID setting can't meet) the requirement of the (these) new processors. However, (Somehow,) this problem can be solved by adding a simple circuit externally. Due to the overlap voltage range between Socket A CPU and that provided by AIC1569A, this method provides a cost-effective solution for Socket A CPU.

VID Configuration

VID pins are used to set the voltage reference for CPU core voltage. This is accomplished by a build-in Digital-to-Analog converter in AIC1569A. There are 5 VID pins named from VID0 to VID4 comprising 32 selections of voltage level. On the other hand, VID definition of Socket A CPU (AMD ThunderBird) also is configured with 5 pins, named VIDx (x=0~4), to define the voltage range from 1.85V to 1.1V. The following table shows both the AIC1569A and ThunderBird CPU voltage levels versus VID setting.

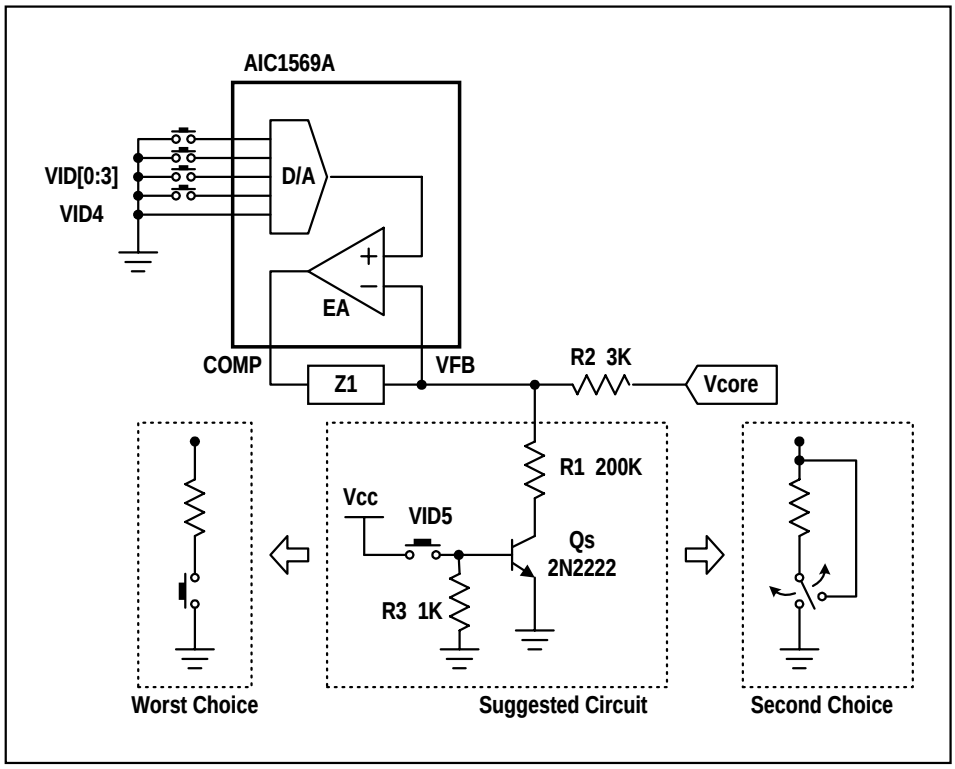
VID[3:0]	V_{CORE} (VID4=0)			V_{CORE} (VID4=1)		
	Socket A	AIC1569A	keep	Socket A	AIC1569A	redefine
0000	1.850	2.05	2.050	1.450	3.5	2.075
0001	1.825	2.00	2.000	1.425	3.4	2.025
0010	1.800	1.95	1.950	1.400	3.3	1.975
0011	1.775	1.90	1.900	1.375	3.2	1.925
0100	1.750	1.85	1.850	1.350	3.1	1.875
0101	1.725	1.80	1.800	1.325	3.0	1.825
0110	1.700	1.75	1.750	1.300	2.9	1.775
0111	1.675	1.70	1.700	1.275	2.8	1.725
1000	1.650	1.65	1.650	1.250	2.7	1.675
1001	1.625	1.60	1.600	1.225	2.6	1.625
1010	1.600	1.55	1.550	1.200	2.5	1.575
1011	1.575	1.50	1.500	1.175	2.4	1.525
1100	1.550	1.45	1.450	1.150	2.3	1.475
1101	1.525	1.40	1.400	1.125	2.2	1.425
1110	1.500	1.35	1.350	1.100	2.1	1.375
1111	1.475	1.30	1.300	No CPU	0V	1.325

By comparing the voltage values in the table, 2 problems are found in the VID mismatch condition. First, voltage range of AIC1569A can not cover the range of Socket A CPU, as mentioned above. Second, for Socket A CPU, the voltage step is 25mV within all range. However, in AIC1569A, voltage step is 100mV within the range from

3.5V to 2.1V and 50mV from 2.1V to 1.3V. You may have noticed that, the difference between 100mV step and 50mV step can be categorized by the VID4 value. Besides, the range of 3.5V~2.1V is not used for Socket A CPU. Thus we can redefine the VID4 pin as a "plus 25mV" function, used within the range of 2.1V to 1.3V. The gray area in the above table is the redefined VID voltage level.

Circuit Modification

How do we apply this redefined VID voltage to practical circuit? The principle is quite simple. Since the VID4 pin of AIC1569A is no longer used, it is connected to ground to keep the reference voltage in the range from 2.05V to 1.3V. The "plus 25mV" function is controlled by the other on/off pin, named VID5. The status of VID5 controls an NPN transistor to enable a resistor that connects between VFB and GND to modify the feedback voltage. Two circuits are shown in the following figure to convey this idea.



In the above figure, "Suggested Circuit" is a little complicated but much more reliable than the "Second Choice". R2 is the original resistor used with Z1 to accomplish the compensation network. Adding an R1 resistor effectively divides the feedback voltage. This also causes the compensator to increase the output voltage. VID5, Grounding of R1 depends on the control circuit which is comprised of R3 and Qs. As VID5 open, Qs is turned off. R1 would not consume any current, voltage on VFB equal to Vcore. And when VID5 closed, Qs is turned on. Voltage on VFB is then no longer Vcore, it gets a smaller Vcore than actual output voltage.

The "Worst Choice" is applied by the same principle as the "Suggested Circuit", but may induce much more noise

and interference while VID5 is open.

The “Second Choice may be the best choice while considering the trade off between cost and noise problem. The advantage of this circuit eliminate the point may induce noise while converter operating. One consideration may be its disadvantage is the switch is not suggested to change while converter operation, the reason is noise may be introduce during the time changing the switch position. With this point of view, change switch position of “Suggested Circuit” can be proceed any time, no matter the converter is operating or not.

Control Circuit Design and Verification

The principle now is very clear, using VID5 to enable the divide circuit. The divided voltage can be calculated by the following equation:

$$V_{FB} = \frac{R1}{R1+R2} \times V_{CORE}$$

By the linear equation shown above, the relation between VFB and Vcore is proportional, not offset. This means we have to choose a proper value of divide resistor (R1) to match the 25mV offset at different reference voltage as possible as we can.

Usually, the R2 value is a parameter decided in compensator design. This simplifies the design of divider. Let’s assume R2 is designed to be 3KΩ, then a mid point is chosen in the VID voltage range. For example, the mid point is 1.7V, and the value of R1 can be calculated as follows.

$$\frac{R1}{R1+R2} = \frac{1.7}{1.7+0.025}$$
$$\Rightarrow \quad R1 = 1.7 \times (3K/0.025) = 204K\Omega$$

Thus, R2 is chosen to be 200KΩ, as we saw in the above schematics. On the other hand, voltage offset under different VID set can also be calculated. The following table shows the calculated value and measured value of the new VID modification circuit.

VID[3:0]	Defined Voltage (V)		Measured Voltage (V)		Deviation (mV)		Voltage Rise (mV)	
	VID5 OFF	VID5 ON	VID5 OFF	VID5 ON	VID5 OFF	VID5 ON	Calculated	Measured
0000	2.050	2.075	2.052	2.083	2	8	30	33
0001	2.000	2.025	2.000	2.031	0	6	30	31
0010	1.950	1.975	1.952	1.981	2	6	29	29
0011	1.900	1.925	1.900	1.929	0	4	28	29
0100	1.850	1.875	1.852	1.880	2	5	27	30
0101	1.800	1.825	1.800	1.827	0	2	27	27
0110	1.750	1.775	1.752	1.778	2	3	26	28
0111	1.700	1.725	1.702	1.727	2	2	25	27
1000	1.650	1.675	1.652	1.677	2	2	24	27
1001	1.600	1.625	1.600	1.624	0	-1	24	24
1010	1.550	1.575	1.552	1.575	2	0	23	25
1011	1.500	1.525	1.501	1.523	1	-2	22	23
1100	1.450	1.475	1.452	1.474	2	-1	21	24
1101	1.400	1.425	1.400	1.421	0	-4	21	21
1110	1.350	1.375	1.352	1.372	2	-3	20	22
1111	1.300	1.325	1.300	1.320	0	-5	19	20

The above table contains the designed and measured data that is tested at no load condition. First column is the set of VID pins (Note VID4 is always connected to ground as shown in above schematics). The second and third columns are the redefined voltage levels. The column with “VID5 on” is always 25mV higher than the column with “VID5 off”. The fourth and fifth columns are the authentic data measured with VID5 off and on, respectively. The sixth and seventh columns show the calculated data of deviation voltage between setting and measured voltage. Obviously the voltage variation with VID5 on turns more dramatic than off, especially at the larger and smaller voltage setting. The last 2 columns are the data from the circuit’s point of view to see the differences between the R2 design and implementation. And the result turns out to be almost the same.

Conclusion

From the test result, some conclusions are made:

1. The redefined VID table can be categorized into 2 parts, the original part of VID4=0, voltage level range is from 2.05V to 1.3V in 50mV step. The other part is an extension from the first part with additional 25mV, which is controlled by a new VID5 bit. Hence, the total provided voltage range is from 2.075V to 1.3V in 25mV step (32 voltage level totally).
2. The extended VID setting can provide the same voltage step as the needs of the Socket A CPU, which is 25mV. However, during the implementation the voltage step is not so accurate. The highest voltage defined in Socket A CPU is 1.85V. That means there are 9 voltage levels (from 2.075V to 1.875V), that are not used. On the other hand, this derived VID setting can only provide the voltage of 1.3V. In other words, the range of 8 voltage levels from 1.275V to 1.1V is not provided to the Socket A CPU.
3. Thus, the valid range provided by the redefined VID table is 1.85V to 1.3V, 23 voltage levels totally. Besides, the “No CPU” defined in Socket A CPU is also not provided.
4. The typical Vcore voltage for Socket A CPU is 1.7V. Therefore, this new derived VID can meet the requirement with no doubt. For the sleeping mode, typically Vcore voltage is 1.3V, also can be provided, but with less flexibility.
5. The voltage level with VID5=1, that is, adding 25mV, had worse voltage deviation than VID5=0, yet still acceptable. The worst case is about 8mV higher at 2.075V and 5mV lower at 1.325V. These values may vary according to case design.
6. Actually, for more cost-effective method, this circuit can simply be further simplified by using R1 and VID5 as the “Second Choice” and “Worse Choice” shown above. This can also achieve the same result but may induce much more noise than original design when the VID5 is open. Please note that lots of care should be taken when implementing this application. Cost difference between “Second Choice” and “Worst Choice” is only a pin.

As the new generation CPU’s performance progressing rapidly, the requirement of power supply specification also challenges the power electronics technology. Although Multi-Phase converter can meet the power requirement for CPU of the next few generations, High cost and complex technology is the price that has to pay at this moment.

This article introduces a cost effectively solution for those users who are not ready to go for the Multi-Phase technology, but have involved with products of K7 Socket

A CPU. By adding a simple circuit (2 resistor, 1 NPN transistor), the old design can then meet the VID requirement of Socket A CPU. It's simple, easy and cost-effective.