SPEC NO: DS-1569A-00

FEATURES

- Compatible with HIP6004.
- Simple Voltage-Mode PWM Control.
- Dual N-Channel MOSFET Synchronous Drive.
- Fast Transient Response.
- ±1% 5-Bit Digital-to-Analog Output Voltage.
- Adjustable Current Limit Without External Sense Resistor.
- Full 0% to 100% Duty Ratio.
- 200KHz Free-Running Oscillator, Programmable up to 350KHz.
- Power-Good Output Voltage Monitor.

APPLICATIONS

- Power Supply for Pentium® II, Power® and Alpha® Microprocessors.
- High-Power 5V to 3.xV DC/DC Regulators.
- Low-Voltage Distributed Power Supplies.

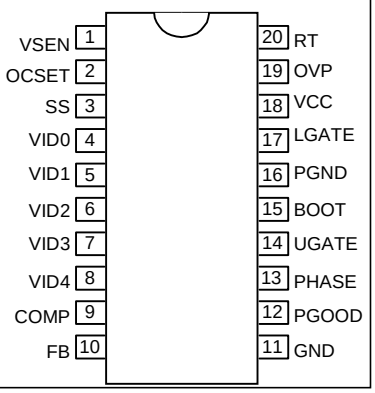
ORDERING INFORMATION

AIC1569A XX

PACKAGE TYPE
S: SMALL OUTLINE

TEMPERATURE RANGE
C: 0°C~70°C

ORDER NUMBER	PIN CONFIGURATION
AIC1569ACS (PLASTIC SO)	TOP VIEW



DESCRIPTION

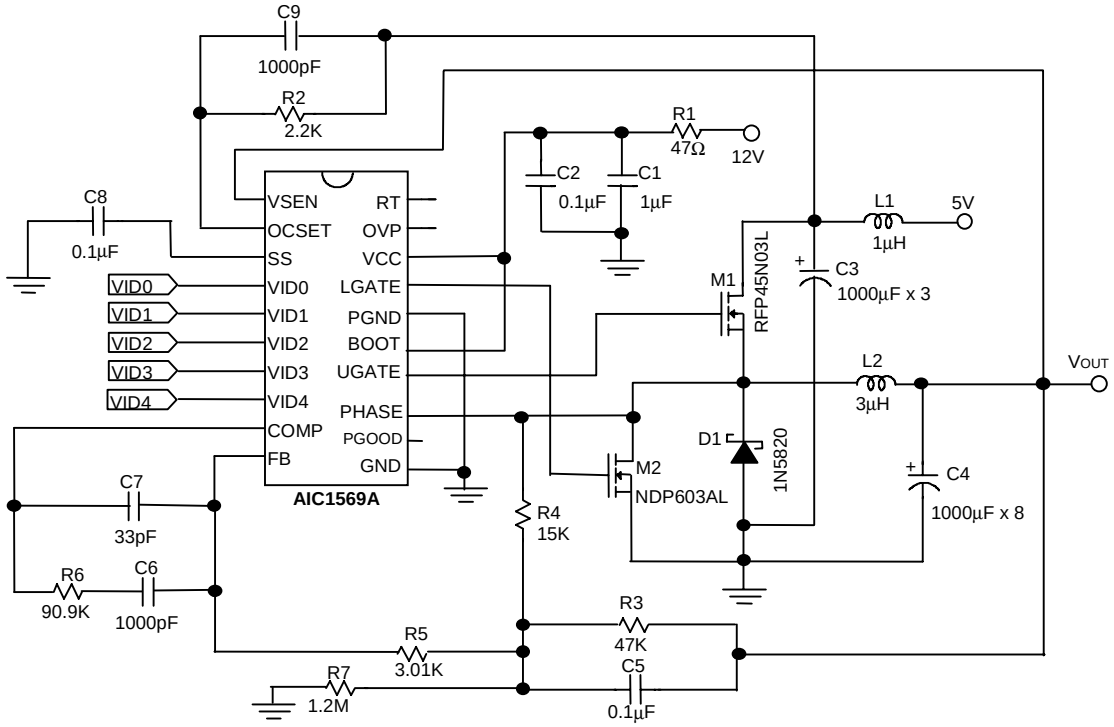
The AIC1569A is a high power, high efficiency switching regulator controller optimized for high performance microprocessor applications. It is designed to drive dual N-channel MOSFETs in a standard synchronous buck topology. Featuring a digitally programmable switching regulator, the AIC1569A includes monitoring and protection capabilities in addition to all the essential synchronous PWM control functions.

The internal 5-bit Digital-to-Analog Converter (DAC) adjusts the output voltage from 2.0V to 3.5V in 0.1V increments and 1.3V to 2.0V in 0.05V increments. The precision reference and voltage-mode control can provide output regulation within ±1% over temperature and line voltage shifts.

The internal oscillator of the AIC1569A free-runs at 200KHz and can be adjusted up to 350KHz. The resulting PWM duty ratio ranges from 0% to 100%. The error amplifier features an 11MHz bandwidth and 6V/μS slew rate, which enables high converter bandwidth for fast transient response.

The AIC1569A provides adjustable over current and short circuit protections. It senses the output current across the on resistance of the upper N-channel MOSFET without an external low value sense resistor. It also monitors the output voltage with a window comparator and issues a power good signal when the output is within 10% of the rated output voltage.

TYPICAL APPLICATION CIRCUIT



DC/DC Converter for Pentium® II V_{CORE}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 15V
Boot Voltage, V_{BOOT} 15V
Input, Output, or I/O Voltage ..... GND -0.3V to VCC+0.3V
ESD Classification ..... Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 12V±10%
Ambient Temperature Range ..... 0°C ~ 70°C
Junction Temperature Range ..... 0°C ~100°C

Thermal Information

Thermal Resistance, θ_{JA} (Typical, Note 1)
SOIC Package ..... 100°C /W
SOIC Package (with 3 in^2 of Copper) ..... 90°C /W
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C ~150°C
Maximum Lead Temperature (Soldering 10 sec) ..... 300°C

Note 1: θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TEST CIRCUIT

Refer to TYPICAL APPLICATION CIRCUIT.

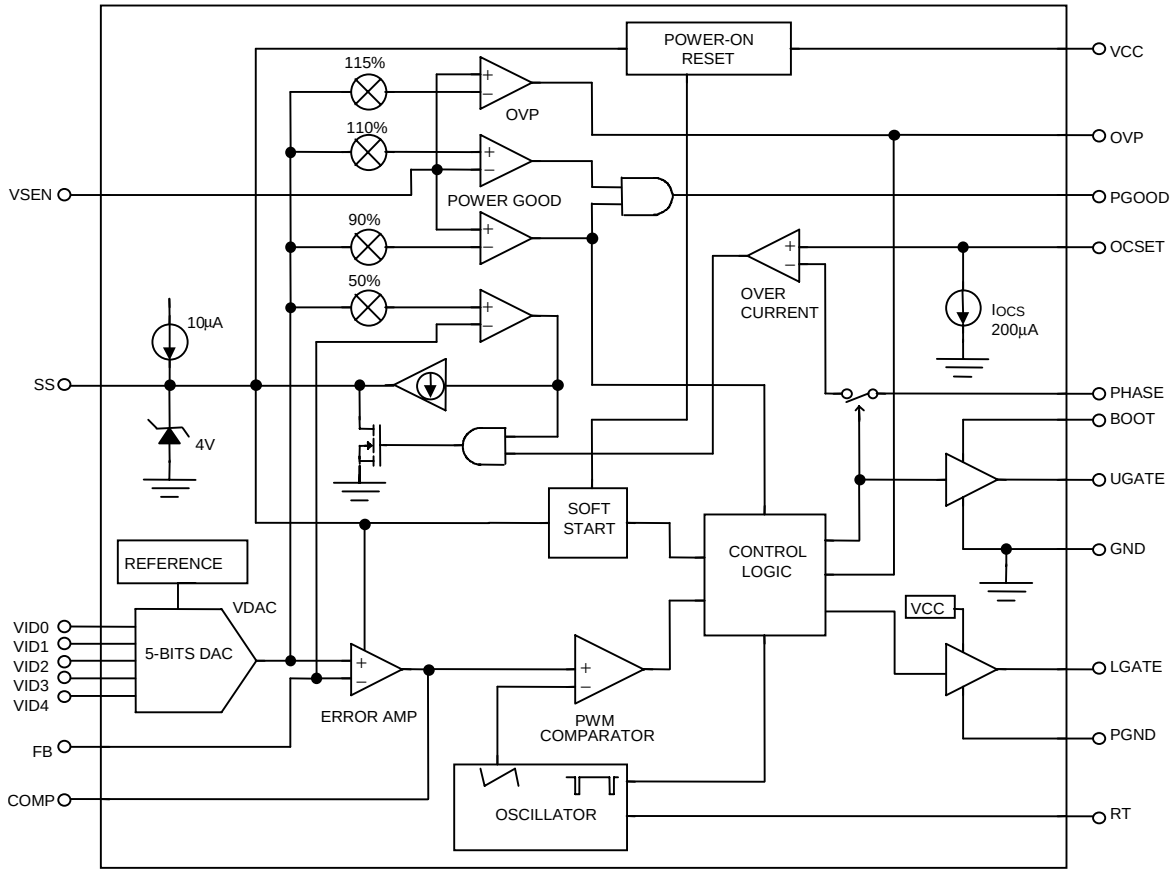
ELECTRICAL CHARACTERISTICS (VCC= 12V, Ta=25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC Supply Current						
Nominal Supply	UGATE Open	I_{VCC}		1	3	mA
Power-On Reset						
V_{CC} Threshold	V_{OCSET}=4.5V		8.2	9.3	10.2	V
Rising V_{OCSET} Threshold				1.26		V
Oscillator						
Free Running Frequency	RT Open		170	200	230	KHz
Total Variation	6KΩ<R_T <200KΩ		-20		+20	%
Ramp Amplitude	RT Open	ΔV_{OSC}		1.5		V_{P-P}
DAC Output Voltage						
DAC Output Voltage Accuracy	VDAC=1.3V~3.5V		-1.0		+1.0	%
Error Amplifier						
DC Gain				76		dB
Gain-Bandwidth Product		GBW		11		MHz
Slew Rate		SR		6		V/μS
Gate Driver						
Upper Gate Source		R_{UGATE}		5.8	12	Ω
Upper Gate Sink		R_{UGATE}		4.4	10	Ω
Lower Gate Source		R_{LGATE}		4.7	12	Ω
Lower Gate Sink		R_{LGATE}		3.0	10	Ω
Protection						
Over-Voltage Trip (V_{VSEN}/VDAC)			106	115	125	%
OCSET Current Source	V_{OCSET}=4.5VDC	I_{OCSET}	170	200	230	μA
OVP Sourcing Current	V_{VSEN}=5.5V, V_{OVP}=0V	I_{OVP}	30			mA
SS Current		I_{SS}		10		μA
SS Voltage under Current Limit	V_{VSEN}=VDAC, V_{OCSET}=5.0V, V_{PHASE}=0V, V_{FB}=VDAC - 50mV			2.0		V
SS Voltage under Hard Current Limit	V_{VSEN}=0, V_{OCSET}=5.0V, V_{PHASE}=0V, V_{FB}=0V			0.7		V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Good						
Upper Threshold (V_{VSEN}/VDAC)	V_{VSEN} Rising		106		114	%
Lower Threshold (V_{VSEN}/VDAC)	V_{VSEN} Falling		84		94	%
Hysteresis (V_{VSEN}/VDAC)	Upper and Lower threshold			2		%
PGOOD Voltage Low	I_{PGOOD}=5mA	V_{PGOOD}		0.5		V

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN 1: VSEN - Converter output voltage sense pin. Connect this pin to the converter output. The PGOOD and OVP comparator circuits use this signal to report output voltage status and perform overvoltage protection function.

PIN 2:OCSET - Current limit sense pin. Connect a resistor R_{OCSET} from this pin to the drain of the external MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCS}), and the external MOSFET on-resistance ($R_{DS(ON)}$) jointly set the over current trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCS} \times R_{OCSET}}{R_{DS(ON)}}$$

If FB pin voltage is sensed to be below 50% of the internal voltage reference VDAC, the over current comparator cycles the soft-start function.

PIN 3:SS - Soft start pin. Connect a capacitor from this pin to ground. An internal 10μA current source provides soft start function for the converter.

PIN 4: VID0
PIN 5: VID1
PIN 6: VID2
PIN 7: VID3
PIN 8: VID4 - 5-bit DAC voltage select pin. TTL inputs used to set the internal voltage reference VDAC. When left open, these pins are internally pulled up to 5V and provide logic ones. The level of VDAC sets the converter output voltage as well as the PGOOD and OVP thresholds.

Table 1 specifies the VDAC voltage for the 32 combinations of DAC inputs.

PIN 9:COMP - External compensation pin. This pin is connected to error amplifier output and PWM comparator. An RC network is connected to FB pin to compensate the voltage-control feedback loop of the converter.

PIN 10:FB - The error amplifier inverting input pin. The FB pin and COMP pin are used to compensate the voltage-control feedback loop.

PIN 11:GND - Signal GND. It also serves as the power GND for the upper gate driver.

PIN 12:PGOOD- Power good indicator pin. PGOOD is an open drain output. This pin is pulled low when the converter output is ±10% out of the VDAC reference voltage.

Table 1. Output Voltage Program

VID4	VID3	VID2	VID1	VID0	VDAC
1	0	0	0	0	3.5V
1	0	0	0	1	3.4V
1	0	0	1	0	3.3V
1	0	0	1	1	3.2V
1	0	1	0	0	3.1V
1	0	1	0	1	3.0V
1	0	1	1	0	2.9V
1	0	1	1	1	2.8V
1	1	0	0	0	2.7V
1	1	0	0	1	2.6V
1	1	0	1	0	2.5V
1	1	0	1	1	2.4V
1	1	1	0	0	2.3V
1	1	1	0	1	2.2V
1	1	1	1	0	2.1V
1	1	1	1	1	2.0V
0	0	0	0	0	2.05V
0	0	0	0	1	2.00V
0	0	0	1	0	1.95V
0	0	0	1	1	1.90V
0	0	1	0	0	1.85V
0	0	1	0	1	1.80V
0	0	1	1	0	1.75V
0	0	1	1	1	1.70V
0	1	0	0	0	1.65V
0	1	0	0	1	1.60V
0	1	0	1	0	1.55V
0	1	0	1	1	1.50V
0	1	1	0	0	1.45V
0	1	1	0	1	1.40V
0	1	1	1	0	1.35V
0	1	1	1	1	1.30V

PIN 13:PHASE - Over current detection pin. Connect the PHASE pin to source of the external MOSFET. This pin detects the voltage drop across the MOSFET $R_{DS(ON)}$ for over-current protection.

PIN 14: UGATE- External MOSFET gate drive pin. Connect UGATE to gate of the external MOSFET.

PIN 15: BOOT - External MOSFET driver power supply pin. To convert 5V main power to V_{CORE} power by driving N-channel MOSFET, supply voltage of no higher than 12V is recommended since the negative power terminal of the internal driver is internally tied to GND.

PIN 16:PGND - Driver power GND pin. PGND should be connected to a low impedance ground plane close to lower N-MOSFET source.

PIN 17:LGATE - Lower N-MOSFET gate driver pin.

PIN 18: VCC - The chip power supply pin. It also serves as power supply for LGATE driver. Recommended supply voltage is 12V.

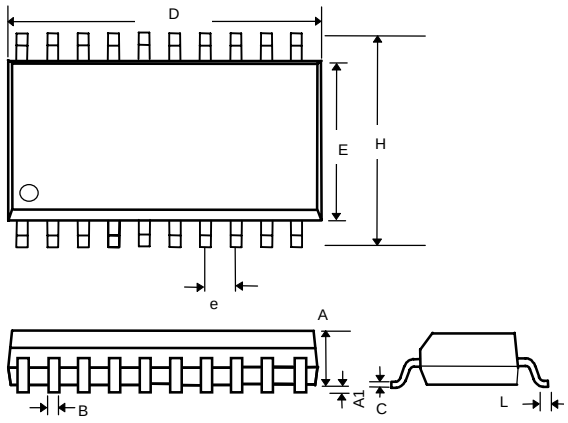
PIN 19:OVP - Over voltage indicator pin. This pin also provides a driver source current to turn on an external SCR in the event of an over voltage condition.

PIN 20: RT - Frequency adjustment pin. Connecting a resistor (RT) from this pin to GND, increase the frequency by the following equation.

$$F_S \cong 200KHz + \frac{5 \times 10^5}{\log R_T}$$

■ PHYSICAL DIMENSIONS

- **20 LEAD PLASTIC SO (300 mil) (unit: mm)**



SYMBOL	MIN	MAX
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27(TYP)	
H	10.00	10.65
L	0.40	1.27