Application Note AN2xxx

TV Based Display System

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Associated Project: Yes
Associated Part Family: CY8C27xxx
PSoC Designer Version: 4.00

Summary

This project shows how easily a TV can be used to display information. RAMDAC like approach is used but even the sync pulses are encoded into the SRAM instead of generating them in hardware. Screen resolution supported is 400H by 148V dots. 18 lines of text with 36 chars each can be displayed with an 8x8 pixel font. Leftover SRAM can be used to store data.

Introduction

Televisions are around us almost everywhere. They are mass produced and therefore inexpensive. They have standard interfaces. Of particular interest are small 6 inch TV sets that are available for about Rs 850 (US $19). These can be used to display information at a much lower cost when compared to LED or LCD display of equivalent size. An experimenters dream come true

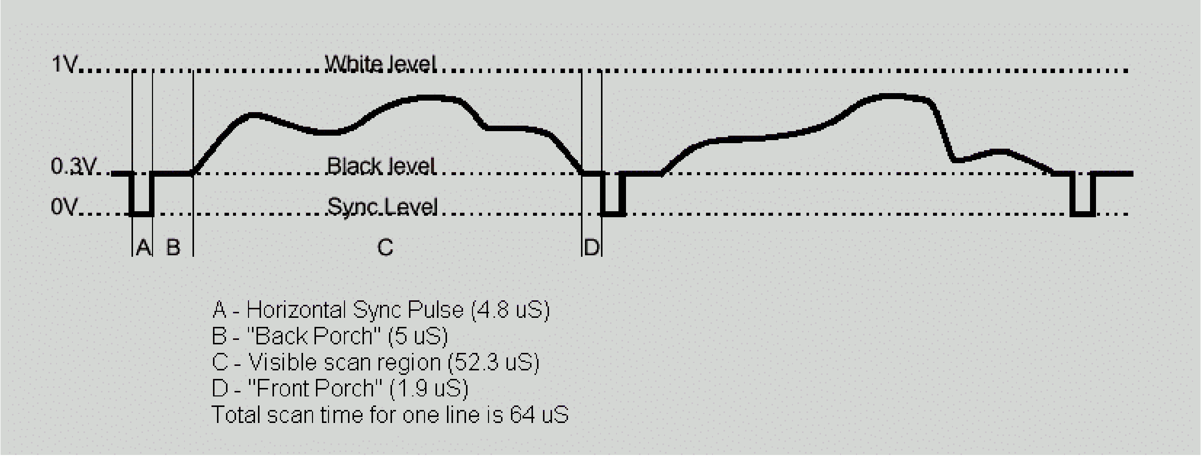
There have been projects before that use TV as a display. They use a very fast (and expensive) MCU to generate all parts of the video signal i.e. video pixels, horizontal sync and vertical sync. Almost all the resources of the MCU are used up in keeping up with the tough timing requirements of a video signal and there is little juice left in the MCU to do anything significant.

This project takes a diametrically opposite approach. The philosophy behind it is that the MCU should compute and all the monotonous tasks are left to memory-DAC subsystem that remembers what the MCU computed and blasts that information to the TV. Memory capacity is cheaper than raw computing power and will remain so. Therefore this circuit uses minimal parts and even the sync pulses (both horizontal & vertical) are encoded into the SRAM. 32 K Byte SRAM chips are about Rs 35 (US $0.75). Thus trying to generate sync pulses with glue logic will be more expensive. Another benefit of soft encoding sync information is the ease in adapting the circuit to support a different video standard. The SRAM area not used for video data can be easily used store information relevant to the task at hand. Address setup and data store operations can be done in 8 bit parallel mode.

PAL Composite Video Signal

This project generates a PAL (phase alteration by line) standard video signal. PAL standard is used in India and is popular in Europe. How a TV displays images is closely related to the structure of the video signal itself. Televisions are raster-scan devices and they trace out their images by quickly moving a single electron beam in a “Z” pattern across the picture tube. The beam starts in the upper left corner of the display, and traces quickly across to the upper right “painting” the first horizontal line of the TV image. When it reaches the right side, the beam turns off, returns to the left side, and paints the second horizontal line. This process continues until all the lines in the TV frame have been painted.

A complete TV image is 625 lines tall and is fully painted 25 times per second. In the early days of TV, it was discovered that the 25Hz refresh rate produced too much flicker to watch comfortably. To reduce this flicker, each full image is split into two fields of 312.5 lines each, and thus fields are displayed at a rate of 50Hz. It permits a higher image repetition frequency without increasing the bandwidth requirements. The first field(odd) contains lines 1,3,5,7… of the original image, and the second field(even) contains lines 2,4,6,8, etc. Each field fills the entire screen, but only paints



A - Horizontal Sync Pulse (4.8 uS)
B - "Back Porch" (5 uS)
C - Visible scan region (52.3 uS)
D - "Front Porch" (1.9 uS)
Total scan time for one line is 64 uS

Figure 1 - Horizontal Scan Line

every other line. For practical purposes, the final 0.5 line of each field can be discarded to make it an even 312 lines/field. Each line takes 64us to paint (15.626 kHz).

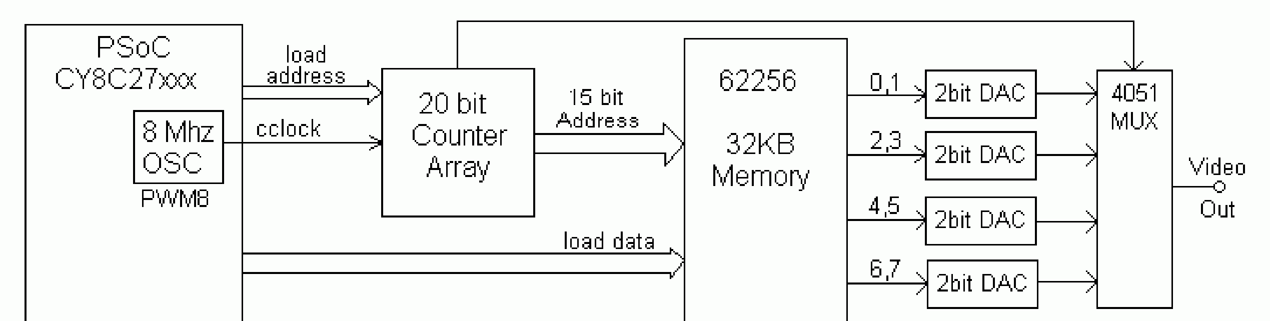
As shown in figure 1, each horizontal scan line consists of H sync pulse, Back Porch and Front Porch. The H sync pulse informs the TV that a new line is about to begin and back porch gives the TV time to position the electron beam to correct position. H sync, back porch and front porch are encoded into the SRAM along with the video data.

A vertical sync pulse informs the TV that a new field is about to begin. The TV then positions the beam to top left corner of the picture tube. There are two types of fields – even and odd. The vertical sync pulses vary slightly according to the field that is to follow. But this circuit makes no distinction between even and odd fields. There is only one field and same video data is sent out for both fields. Hence vertical sync pulse is also same and is generated by sending 4 lines of inverted H sync with blank video followed by 4 blank video lines.

Implementation

Each video frame is made of 625 lines with 312.5 lines each in the even and odd fields. But both fields are treated as same and two consecutive lines are also same. Thus 312 lines divided by 2 gives 156 lines. Out of 156 these lines, 8 are used for vertical sync. This leaves 148 vertical lines. TV sets are unable to show lines at the beginning of the field, so more lines may not be visible.

Each video line is divided into 512 locations. First 8 are part of front porch, next 40 are H sync and the next 60 represent back porch. Video data is encoded in the next 400. The remaining 4 are part of front porch. Each screen pixel is allocated 2 bits giving 4 possible voltage levels. 00 is sync level, 01 is black level, 10 is a shade of grey and 11 represents white. Consider a memory range from location 0000h to 01FFFh of 512 bytes. The bits 0 & 1 of 0000h represent video pixel 0 on line 0, bits 2 & 3 represent video pixel 0 on line 1,



Block Diagram

bits 4 & 5 represent video pixel 0 on line 2 and lastly bits 6 & 7 of 0000h represent pixel 0 on line 3. Thus the memory range 0000h to 0200h covers 4 lines – line 0, line 1, line 2 & line 3. Each consecutive 512 byte memory range holds data for corresponding 4 lines.

Thus the screen resolution is 400 horizontal dots by 148 vertical dots.

Video Memory Map:

Memory Addresses	Line Numbers
0000h - 01FFh	0 - 3
0200h - 03FFh	4 - 7
0400h - 05FFh	8 - 11
……	……
1400h - 15FFh	40 - 43
…….	…….
2800h - 29FFh	80 - 83
……...	…….
4A00h - 4BFFh	148 - 151
4C00h - 4DFFh	152 - 155

Line duration in PAL video standard is 64 microseconds. To send 512 values in 64 uS the data rate required is 8 MHz. This 8 MHz signal is generated by a PSoC digital block configured as a 50% duty cycle 8 bit Pulse Width Modulator.

The circuit has a counter array followed by a SRAM chip. The counter array is formed by cascading five 74LS163 4 bit pre-settable synchronous edge-triggered binary counters. This counter array provides the address to the SRAM. The SRAM outputs the data at that address to 2-bit DAC's (Digital to Analog converters) made by using resistors of 480 ohms and 2200 ohms. The DAC's output is a voltage level between 0 and 1 volt which is required to drive the TV. Since each byte has data for 4 pixels, the output of the 4 DACs is sent to 4051 MUX which selects the output value depending on the line being displayed.

The circuit has 2 modes of operation – TV mode and MCU mode.

In the TV mode the PSoC is completely free do any task and there is no computation load or interrupts bothering it. Only resource required is a 8 MHz clock signal to the counter array generated by a PWM digital block. In the MCU mode the PSoC takes a more direct control and it can set addresses, read & write data, reset counter state etc.

The number of PSoC port lines used is 15. Port 2 is used as an 8 bit port to set counter state and read & write data from SRAM. Seven Port 1 lines are used individually as control signals to manipulate the circuit operation.

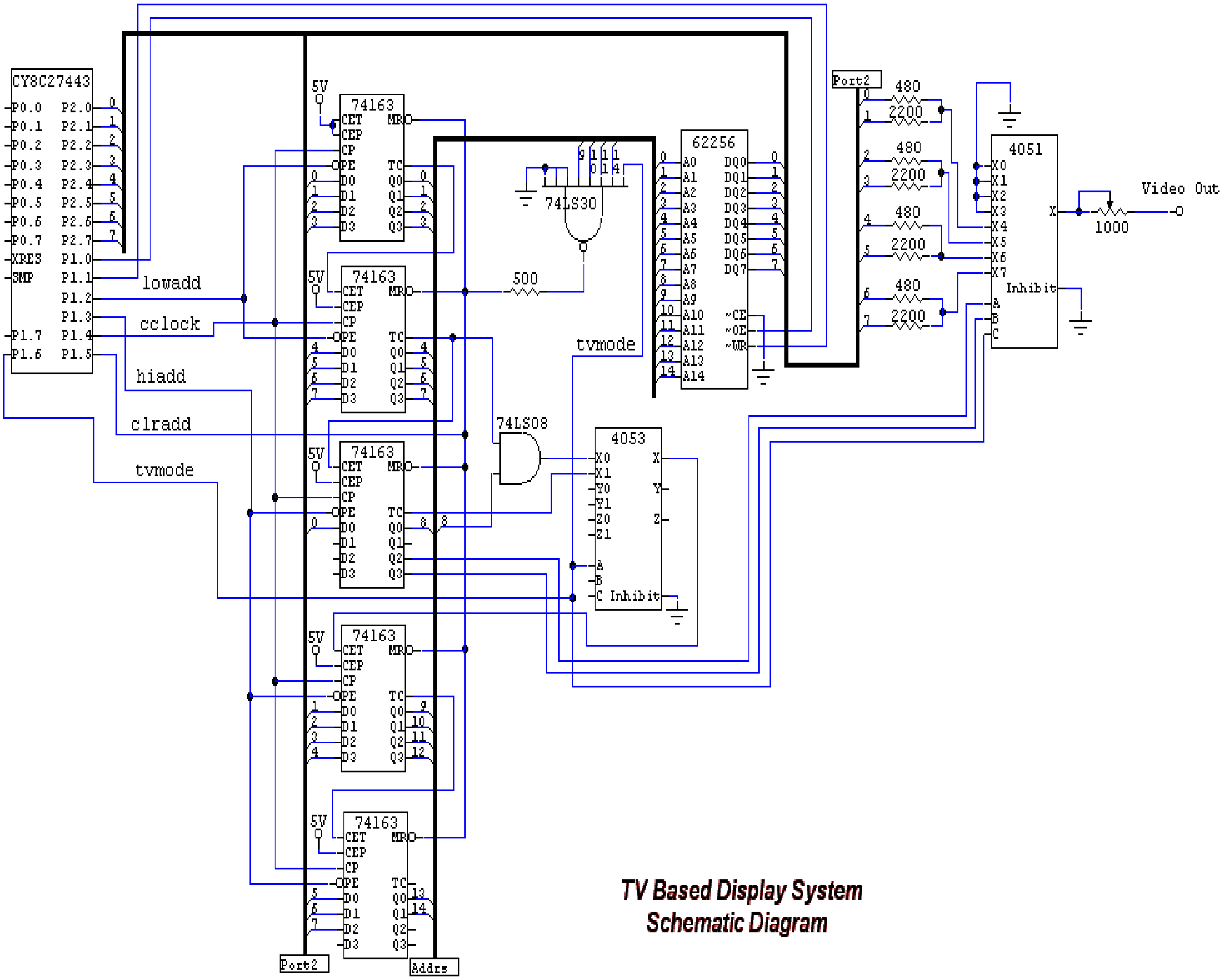
PORT 1 Description:

Line no	Name	Description
P1.0	memoe	Enable SRAM output
P1.1	memwr	Write data into SRAM
P1.2	lowadd	Set lower 8 bits of counter array (i.e. address)
P1.3	hiadd	Set higher 8 bits of counter array (i.e. address)
P1.4	cclock	Clock signal to the counter array (8 MHz in TV mode)
P1.5	clradd	Reset counter array
P1.6	tvmode	Set mode of operation to TV mode or MCU mode

In the TV mode of operation, the PSoC gives out an 8MHz clock signal to the counter array. The counters count the pulses and generate the address signals for the SRAM. The counter array is configured as 20 bit binary counter. The first 9 bits are used as address lines A0 – A8 for the SRAM. 2^9 = 512 bytes i.e. first 9 bits cover the width of the screen. The 10th bit is ignored because 2 consecutive lines are treated as same. The bit no 11 and 12 control the MUX and select one out of four lines. The next 6 bits are used as address lines A9 – A14 for the SRAM. These select the line number. The last 2 bits are not used for now but can be used to increase the screen resolution by using a larger SRAM.

The 8bit data output from SRAM is converted to analog voltage level by four 2-bit resistive DACs. The 4051 MUX selects one of these and sends it as output to the TV. A variable resistance connected to the MUX output can help in varying the voltage level to suit different TV sets.

After 156 lines (actually one field of 312 lines) have been displayed, the counter state is 4E00h. This state is decoded by 74LS30 8-input NAND gate and it resets the counters through a 500 ohm resistor. This resistor ensures that the PSoC has no problem in driving this signal in MCU mode and also that the gate is not damaged by the superior drive power of the PSoC MCU.



TV Based Display System
Schematic Diagram

In the MCU mode of operation the PSoC takes complete control of the circuit. The cclock (P1.4) line is internally disconnected from the PWM block and is now used as a standard port line. The TV mode (P1.6) signal is driven low. This reconfigures the counter array and it becomes a 17 bit binary counter. The counter outputs 0 – 8 and 12 – 17 are used as A0 – A14 for SRAM. Notice that 4053 MUX is used to select input to CET pin of the 4th counter. This is done to prevent spurious dots from appearing on the screen, which can occur due to gate delay if AND gates are used. Driving tvmode low also disables the address decoder 74LS30 and TV output is now connected to ground by the 4051 MUX.

To reset the counters clradd(P1.5) signal is made low (active) and cclock line toggled once. The clradd signal is then returned to its inactive high state.

To set lower 8 bits of address Port 2 is loaded with the required value, lowadd (P1.2) signal is made low (active) and the cclock line toggled once. The lowadd signal is then returned to its inactive high state.

Similarly to set upper 8 bits of address Port 2 is loaded with the required value, hiadd (P1.3) signal is made low (active), and the cclock toggled once. The hiadd signal is then returned to its inactive high state.

Data is written in SRAM by setting the required address as described above. Then Port 2 is loaded with the required value and memwr (P1.1) line is toggled once. If consecutive address locations are to be written, address can be incremented by toggling the cclock line. This simplifies and speeds up the write operation.

Data is read from SRAM by setting the required address as described above. Then memoe(P1.0) line is made low (active) and data is read from Port2 which has been set to digital input mode. The memoe signal is then returned to its inactive high state.

12800 bytes of memory from 4E00h to 7FFFh can be used to store data because they are not used for video information.

Writing Text on TV Screen

The file font.h contains 8x8 bitmaps for 95 characters of the ASCII set. The sequence of characters in font.h is same as ASCII. The first 32 characters of the ASCII set are not included.

Each character is displayed on 8 lines. So on 148 lines a maximum of 18 text lines can be displayed. This number can be further limited by the TV used because top and bottom lines are cut by TV sets. The screen width is 400 pixels. So the maximum of 40 characters per line can be displayed. The software puts a gap of 2 pixels between two characters so that each character takes 10 pixels. But TV sets cut pictures on the sides also limiting the maximum displayable characters to 35 or 36.

The text can be displayed in two “colours” – grey and white. If colour parameter to wrttxt() or wrtchr() function is set to 1, then grey colour is used and white colour is used if parameter is 2.

A character can be “erased” by writing a blank i.e. space character (ASCII char no 32) in its position. Writing multiple blanks will erase larger areas of the screen.

I hope that you will enjoy painting your data on the vivid canvas that a TV screen is.

<u>List of IC’s in the design:</u>

1 x CY8C27443	- PSoC on Invention Board
5 x 74LS163	- Synchronous Counters
1 x 74LS30	- 8 input NAND gate
1 x 74LS08	- 2 input AND gate
1 x 62256	- 32 K Byte SRAM
1 x CD4053	- Triple 2 channel analog MUX
1 x CD4051	- 8 channel analog MUX

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